TRITON™ LP

The next generation XScale™ based TRITON™ LP module is specially designed for mobile battery based solutions. Equipped with specialized ultra-low-power components, like mobile SDRAMs and a low-power Ethernet controller, extreme low power consumption is achieved in sleep-mode. By programmable core-power generation and clock-rate selection, a flexible control of the total power-consumption for any application is possible.

TRITON™ is a complete computer implemented on a board smaller than a credit card, and ready to be designed into your embedded system. TRITON™ includes a 400MHz Intel® XScale™ processor, SDRAM and Flash memory. The integrated LCD-controller enables direct connection of a LCD screen. Despite that powerful features, the module occupies an area of just 67,6 x 36,6 mm. With the alternatively usable ultra-low-profile connectors (200 pins), a max. height of 7,3 mm is possible.

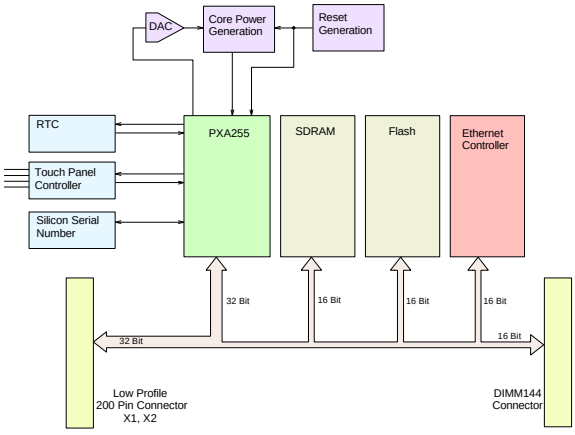
XScale™

Intel's new XScale™ processor family increases efficiency and decreases processor power consumption. The Intel® XScale™ microarchitecture is based on the solid and widely used foundation of the Intel® StrongARM technology. Optimized for the development of highly efficient mobile internet devices, and for network infrastructure applications, Intel® StrongARM and Intel® XScale™ are compatible with the ARM architecture, which in turn guarantees the compatibility of software solutions.
Turbo mode enables the processor to scale its performance as high or as low as necessary in a single clock cycle, which helps conserve battery lifetime while still meeting performance requirements. In addition, the new micro-power management features for these devices allow the processors to potentially use less than half the power at the same performance levels of the Intel StrongARM SA-1110 applications processor.

Redboot™

TRITON™ is delivered with pre-installed Redboot™ firmware. Redboot™ supports several low-level-debugging options and file download via serial XModem or TFTP via ethernet. These files can additionally be stored into the permanent flash-memory to be started by command or power-on.

Features:

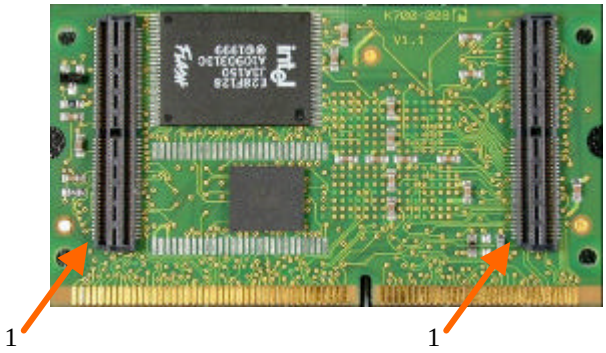


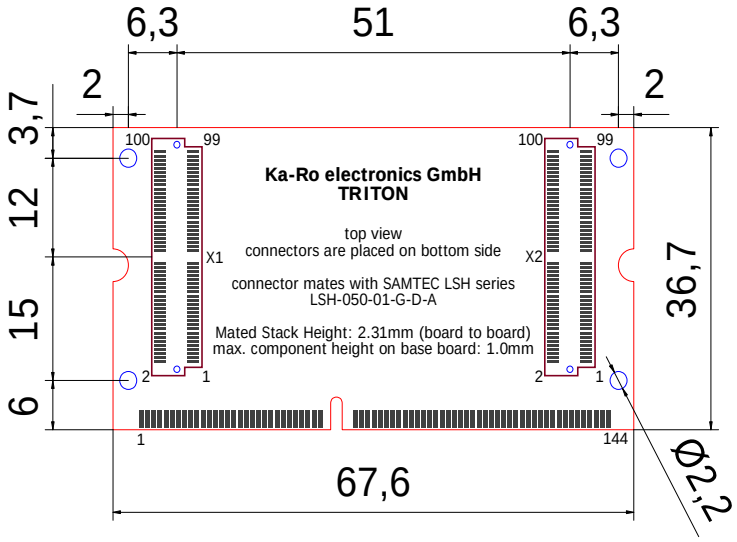
- Intel XScale™ PXA255 (200/300/400MHz)
- 16/32 MByte Low Power SDRAM (8Mx16, 16Mx16)
- 8/16 Mbyte Flash memory (8Mx16)
- Reset logic, I²C, JTAG interface
- 3 asynchronous, 1 synchronous serial interfaces
- LCD controller
- PC-CARD / compact-flash interface
- Single 3,3V power supply
- Programmable Core-voltage generation
- Redboot™ firmware

- 10 MBit/s Ethernet controller CS8900A onboard
- Unique silicon serial number DS2430A
- I²S, AC97 interface available
- Alternatively robust Ultra-Low-Profile (200 pins) or standard DIMM (144 pins) mounting
- Ultra-Low-Profile overall dimensions 67,6 x 36,6 x 7,3mm (mounted on baseboard)
- Complete 32-bit memory interface available
- Min. power consumption 2mW (standby, 16MB SDRAM)
- I²C RTC DS1339 onboard with separate power supply pin
- I²C Touch Screen Controller TSC2003 onboard (optional)

top view

rear view – LTH connectors used on TRITON





Ordering information

Order Number (Valid Combination)	PXA255	CS8900A	Touch Screen Controller	SDRAM	Flash	SAMTEC Expansion Connector
TRITON-LP/300/16S/16F/ETN/EXP/I	300MHz	x	-	16MB	16MB	x

The order number is formed by a combination of the elements below. Other Valid Combinations planned to be supported in volume. Consult the sales office to confirm availability of specific combinations and to check on newly released combinations.

TRITON-LP/ 300/ 16S/ 16F/ ETN/ TS/ EXP / I

I: Industrial Temp. (-40°C to 85°C) **C:** Commercial (0°C-70°C)

EXP: Samtec Expansion Connector

TS: Touch Screen Controller

ETN: CS8900A

8F: 8Mbyte Intel Strata-Flash / **16F**: 16Mbyte Intel Strata-Flash

16S: 16Mbyte SDRAM / **32S**: 32Mbyte SDRAM

200: 200MHz / **300**: 300MHz / **400**: 400MHz

X1 connector pinout

Pin	Signal	Description	Pin	Signal	Description
1	BITCLK / GPIO28	AC97 Audio Port bit clock (output)	2	ETN_Tx-	Ethernet Transmit Output, negative
3		reserved for future use	4	ETN_Tx+	Ethernet Transmit Output, positive
5	SDATA_IN1 / GPIO32	AC97 Audio Port data in (input)	6	ETN_Rx-	Ethernet Receive Input, negative
7	ACRESET#	AC97 Audio Port reset signal (output)	8	ETN_Rx+	Ethernet Receive Input, positive
9	SDATA_OUT / GPIO30	AC97 Audio Port data out (output)	10	ETNLED1	Ethernet LED 1
11	GND	GND	12	GND	GND
13	SYNC / GPIO31	AC97 Audio Port sync signal (output)	14	ETNLED2	Ethernet LED 2
15	SDATA_IN0 / GPIO29	AC97 Audio Port data in (input)	16	PWM1 / GPIO17	Pulse Width Modulation channel 1
17	PWM0 / GPIO16	Pulse Width Modulation channel 0	18	SSPTXD / GPIO25	Synchronous Serial Port Transmit Pin
19	SSPRXD / GPIO26	Synchronous Serial Port Receive Pin	20	SSPSFRM / GPIO24	Synchronous Serial Port Frame Pin
21	SSPSCLK / GPIO23	Synchronous Serial Port Clock Pin	22	TMS	JTAG Test Mode Select
23	TDO	JTAG Test Data Out	24	TRST#	JTAG Test Reset
25	TCK	JTAG Test Clock	26	RESET_IN#	Reset Input
27	TDI	JTAG Test Data In	28	RESET_OUT#	Reset Output
29	GND	GND	30	GND	GND
31	BATT_FAULT	Battery Fault, switch into sleepmode	32	RTC_VCC	Standby Supply
33	GPIO0	General Purpose I/O-Pin	34	BTRXD / GPIO42	Bluetooth UART Receive Pin (3,3V-Level)
35	GPIO1	General Purpose I/O-Pin	36	BTTXD / GPIO43	Bluetooth UART Transmit Pin (3,3V-Level)
37	PIOIS16# / GPIO57	PCMCIA Interface I/O select 16 Bit	38	BTCTS / GPIO44	Bluetooth UART Clear to Send (3,3V-Level)
39	PWAIT# / GPIO56	PCMCIA Interface Wait	40	BTRTS / GPIO45	Bluetooth UART Ready to Send (3,3V-Level)
41	PSKTSEL / GPIO54	PCMCIA Interface Socket Select	42	FFRXD / GPIO34	Full Function UART Peceive Pin (3,3V-Level)
43	PIOW# / GPIO51	PCMCIA Interface I/O Write	44	FFTXD / GPIO39	Full Function UART Transmit (3,3V-Level)
45	PCE2# / GPIO53	PCMCIA Interface High Byte Enable	46	FFDCD / GPIO36	Full Function UART Carrier Detect (3,3V)
47	PIOR# / GPIO50	PCMCIA Interface I/O Read	48	FFCTS / GPIO35	Full Function UART Clear To Send (3,3V)
49	+3,3V	power supply	50	+3,3V	power supply
51	+3,3V	power supply	52	+3,3V	power supply
53	TSMY	Touch Screen, neg Y	54	FFRI / GPIO38	Full Function UART Ring Ind. (3,3V Level)
55	TSMX	Touch Screen, neg X	56	FFDSR / GPIO37	Full Function UART Data Set Rdy. (3,3Vl)
57	TSPY	Touch Screen, pos Y	58	FFDTR / GPIO40	Full Function UART Data Term. Rdy. (3,3V)
59	TSPX	Touch Screen, pos X	60	FFRTS / GPIO41	Full Function UART Rdy. To Send (3,3V)
61	GND	GND	62	GND	GND
63	USB_N	USB-Port neg. Pin (3,3V-Level)	64	L_BIAS / GPIO77	LCD bias drive
65	USB_P	USB-Port pos. Pin (3,3V-Level)	66	LDD13 / GPIO71	LCD interface data bus
67	SDA	I2C data signal	68	LDD9 / GPIO67	LCD interface data bus
69	SCL	I2C clock signal	70	LDD3 / GPIO61	LCD interface data bus
71	L_LCLK / GPIO75	LCD Interface Line Clock	72	LDD8 / GPIO66	LCD interface data bus
73	LDD1 / GPIO59	LCD interface data bus	74	L_PCLK / GPIO76	LCD Interface Pixel Clock
75	GND	GND	76	GND	GND
77	LDD2 / GPIO60	LCD interface data bus	78	LDD11/ GPIO69	LCD interface data bus
79	L_FCLK / GPIO74	LCD Interface Frame Clock	80	LDD12 / GPIO70	LCD interface data bus
81	LDD5 / GPIO63	LCD interface data bus	82	LDD10 / GPIO68	LCD interface data bus
83	LDD14 / GPIO72	LCD interface data bus	84	LDD15 / GPIO73	LCD interface data bus
85	LDD0 / GPIO58	LCD interface data bus	86	LDD7 / GPIO65	LCD interface data bus
87	GND	GND	88	GND	GND
89	LDD6 / GPIO64	LCD interface data bus	90	IR_RXD / GPIO46	IrDA Receive Pin (3,3V- Level)
91	LDD4 / GPIO62	LCD interface data bus	92	IR_TxD / GPIO47	IrDA Transmit Pin (3,3V-Level)
93	PCE1# / GPIO52	PCMCIA Interface Low Byte Enable	94	GPIO11	General Purpose I/O-Pin
95	POE# / GPIO48	PCMCIA Interface Output Enable	96	GPIO10	General Purpose I/O-Pin
97	PREG# / GPIO55	PCMCIA Interface Register Select	98	PWE# / GPIO49	PCMCIA Interface Write Enable
99	GND	GND	100	GND	GND

X2 connector pinout

Pin	Signal	Description	Pin	Signal	Description
1	GND	GND	2	GND	GND
3	RD/WR#	Read not Write	4	WE#	Memory Write Enable
5	nSDCKE1	SDRAM device clock enable	6	OE#	Memory Output Enable
7	nSDCKE0	SMROM or synchronous Flash clock enable	8	RDY	Ready Pin (Wait)
9	SDCLK0	SMROM or synchronous Flash clock	10	nCS2	Chip Select
11	GND	GND	12	GND	GND
13	SDCLK2	SDRAM banks 2/3 clock	14	nCS3	Chip Select
15	nSDCS3	SDRAM Chip Select for banks 3	16	nCS4	Chip Select
17	nSDCS2	SDRAM Chip Select for banks 2	18	nCS5	Chip Select
19	nSDCAS	SDRAM column address strobe (CAS)	20	MD16	memory data bus
21	GND	GND	22	GND	GND
23	nSDRAS	SDRAM row address strobe (RAS)	24	MD17	memory data bus
25	DQM3	data output byte enable 3	26	MD18	memory data bus
27	DQM2	data output byte enable 2	28	MD19	memory data bus
29	DQM1	data output byte enable 1	30	MD20	memory data bus
31	DQM0	data output byte enable 0	32	MD21	memory data bus
33	GND	GND	34	GND	GND
35	MA25	Memory address bus	36	MD22	memory data bus
37	MA24	Memory address bus	38	MD23	memory data bus
39	MA23	Memory address bus	40	MD24	memory data bus
41	MA22	Memory address bus	42	MD25	memory data bus
43	GND	GND	44	GND	GND
45	MA21	Memory address bus	46	MD26	memory data bus
47	MA20	Memory address bus	48	MD27	memory data bus
49	MA19	Memory address bus	50	MD28	memory data bus
51	MA18	Memory address bus	52	MD29	memory data bus
53	GND	GND	54	GND	GND
55	MA17	Memory address bus	56	MD30	memory data bus
57	MA16	Memory address bus	58	MD31	memory data bus
59	DREQ0 / GPIO20	DMA Request Channel 0	60	DREQ1 / GPIO19	DMA Request Channel 1
61	MA15	Memory address bus	62	MD15	memory data bus
63	MA14	Memory address bus	64	MD7	memory data bus
65	MA13	Memory address bus	66	MD14	memory data bus
67	MA12	Memory address bus	68	MD6	memory data bus
69	GND	GND	70	GND	GND
71	MA11	Memory address bus	72	MD13	memory data bus
73	MA10	Memory address bus	74	MD5	memory data bus
75	MA9	Memory address bus	76	MD12	memory data bus
77	MA8	Memory address bus	78	MD4	memory data bus
79	GND	GND	80	GND	GND
81	MA7	Memory address bus	82	MD11	memory data bus
83	MA6	Memory address bus	84	MD3	memory data bus
85	MA5	Memory address bus	86	MD10	memory data bus
87	MA4	Memory address bus	88	MD2	memory data bus
89	GND	GND	90	GND	GND
91	MA3	Memory address bus	92	MD9	memory data bus
93	MA2	Memory address bus	94	MD1	memory data bus
95	MA1	Memory address bus	96	MD8	memory data bus
97	MA0	Memory address bus	98	MD0	memory data bus
99	GND	GND	100	GND	GND

DIMM144 connector pinout

Pin	Signal	Description	Pin	Signal	Description
1	ETN_Rx+	* Ethernet Receive Input, positive	73	LDD5 / GPIO63	LCD interface data bus
2	ETN_Tx+	* Ethernet Transmit Output, positive	74	LDD2 / GPIO60	LCD interface data bus
3	ETN_Rx-	* Ethernet Receive Input, negative	75	LDD3 / GPIO61	LCD interface data bus
4	ETN_Tx-	* Ethernet Transmit Output, negative	76	LDD0 / GPIO58	LCD interface data bus
5	ETNLED1	* Ethernet LED 1	77	LDD1 / GPIO59	LCD interface data bus
6	FFRI / GPIO38	* Full Function UART Ring Ind. (3,3V)	78	GND	Ground
7	ETNLED2	* Ethernet LED 2	79	PWE# / GPIO49	PCMCIA Interface Write Enable
8	SDATA_IN0 / GPIO29	* AC97 Audio Port data in (input)	80	POE# / GPIO48	PCMCIA Interface Output Enable
9	SDATA_OUT / GPIO30	* AC97 Audio Port data out (output)	81	PIOW# / GPIO51	PCMCIA Interface I/O Write
10	SDATA_IN1 / GPIO32	* AC97 Audio Port data in (input)	82	PIOR# / GPIO50	PCMCIA Interface I/O Read
11	ACRESET#	* AC97 Audio Port reset signal (output)	83	PWAIT# / GPIO56	PCMCIA Interface Wait
12	BITCLK / GPIO28	* AC97 Audio Port bit clock (output)	84	PIOIS16# / GPIO57	PCMCIA Interface I/O select 16 Bit
13	SYNC / GPIO31	* AC97 Audio Port sync signal (output)	85	PREG# / GPIO55	PCMCIA Interface Register Select
14	DQM0	* data output byte enable 0	86	PSKTSEL / GPIO54	PCMCIA Interface Socket Select
15	DQM1	* data output byte enable 1	87	PCE1# / GPIO52	PCMCIA Interface Low Byte Enable
16	SDCLK0	* SMROM or synchronous Flash clock	88	PCE2# / GPIO53	PCMCIA Interface High Byte Enable
17	GND	GND	89	+3,3V	power supply
18	GND	GND	90	+3,3V	power supply
19	TMS	JTAG Test Mode Select	91	D14	memory data bus
20	TCK	JTAG Test Clock	92	D15	memory data bus
21	TRST#	JTAG Test Reset	93	D12	memory data bus
22	TDO	JTAG Test Data Out	94	D13	memory data bus
23	RESET_INPUT#	Reset Input	95	D10	memory data bus
24	TDI	JTAG Test Data In	96	D11	memory data bus
25	RESET_OUT#	Reset Output	97	D8	memory data bus
26	L_BIAS / GPIO77	LCD bias drive	98	D9	memory data bus
27	BT_RxD / GPIO42	Bluetooth UART Receive Pin (3,3V-Level)	99	D6	memory data bus
28	BATT_FAULT	Battery Fault, switch into sleepmode	100	D7	memory data bus
29	BT_TxD / GPIO43	Bluetooth UART Transmit Pin (3,3V-Level)	101	D4	memory data bus
30	IR_RXD / GPIO46	IrDA Receive Pin (3,3V- Level)	102	D5	memory data bus
31	FF_RxD / GPIO34	Full Function UART Peceive (3,3V-Level)	103	D2	memory data bus
32	IR_TxD / GPIO47	IrDA Transmit Pin (3,3V-Level)	104	D3	memory data bus
33	FF_TxD / GPIO39	Full Function UART Transmit (3,3V-Level)	105	D0	memory data bus
34	USB_N	USB-Port neg. Pin (3,3V-Level)	106	D1	memory data bus
35	+3,3V	Power supply	107	GND	Ground
36	RTC_VCC	* RTC Supply	108	GND	Ground
37	SDA	I2C data signal	109	RDY / GPIO18	Ready Pin (Wait)
38	USB_P	USB-Port pos. Pin (3,3V-Level)	110	WE#	Memory Write Enable
39	SSP_TxD / GPIO25	Synchronous Serial Port Transmit Pin	111	RD/WR#	Read not Write
40	SCL	I2C Clock Signal	112	OE#	Memory Output Enable
41	SSP_CLK / GPIO23	Synchronous Serial Port Clock Pin	113	GND	Ground
42	SSP_FRM / GPIO24	Synchronous Serial Port Frame Pin	114	CS5# / GPIO33	Chip Select
43	DREQ0 / GPIO20	DMA Request Channel 0	115	CS4# / GPIO80	Chip Select
44	SSP_RxD / GPIO26	Synchronous Serial Port Receive Pin	116	CS3# / GPIO79	Chip Select
45	FF_DCD / GPIO36	Full Function UART Carrier Detect (3,3V)	117	CS2# / GPIO78	Chip Select
46	DREQ1 / GPIO19	DMA Request Channel 1	118	nSDCAS	* SDRAM column address strobe (CAS)
47	FF_DTR / GPIO40	Full Function UART Data Term. Rdy. (3,3V)	119	A25	Memory address bus
48	FF_DSR / GPIO37	Full Function UART Data Set Rdy. (3,3V)	120	A24	Memory address bus
49	FF_RTS / GPIO41	Full Function UART Rdy. To Send (3,3V)	121	A23	Memory address bus
50	FF_CTS / GPIO35	Full Function UART Clear To Send (3,3V)	122	A22	Memory address bus
51	BT_RTS / GPIO45	Bluetooth UART Ready To Send Pin (3,3V)	123	A21	Memory address bus
52	BT_CTS / GPIO44	Bluetooth UART Clear To Send Pin (3,3V)	124	A20	Memory address bus
53	GPIO10	General Purpose I/O-Pin	125	A19	Memory address bus
54	GPIO11	General Purpose I/O-Pin	126	A18	Memory address bus
55	LDD14 / GPIO72	LCD interface data bus	127	A17	Memory address bus
56	LDD15 / GPIO73	LCD interface data bus	128	A16	Memory address bus
57	LDD12 / GPIO70	LCD interface data bus	129	A15	Memory address bus
58	LDD13 / GPIO71	LCD interface data bus	130	A14	Memory address bus
59	LDD10 / GPIO68	LCD interface data bus	131	A13	Memory address bus
60	LDD11/ GPIO69	LCD interface data bus	132	A12	Memory address bus
61	LDD8 / GPIO66	LCD interface data bus	133	A11	Memory address bus
62	LDD9 / GPIO67	LCD interface data bus	134	A10	Memory address bus
63	GPIO0	General Purpose I/O-Pin	135	A9	Memory address bus
64	GPIO1	General Purpose I/O-Pin	136	A8	Memory address bus
65	GND	Ground	137	A7	Memory address bus
66	GND	Ground	138	A6	Memory address bus
67	L_FCLK / GPIO74	LCD Interface Frame Clock	139	A5	Memory address bus
68	L_LCLK / GPIO75	LCD Interface Line Clock	140	A4	Memory address bus
69	L_PCLK / GPIO76	LCD Interface Pixel Clock	141	A3	Memory address bus
70	LDD6 / GPIO64	LCD interface data bus	142	A2	Memory address bus
71	LDD7 / GPIO65	LCD interface data bus	143	A1	Memory address bus
72	LDD4 / GPIO62	LCD interface data bus	144	A0	Memory address bus

(* Modified TRITON pinout used on this module)

Memory-Map

In the Intel PXA255 Developer's Manual you will find the memory map of the PXA250 processor on pages 2-28 and 2-29. The TRITON-ETN uses the memory as follows:

```
0xA000 0000 - 0xA0FF FFFF     16 MBytes SDRAM

0x0400 0310 – 0x07ff ffff     Reserved by the Ethernet Controller
0x0400 0300 - 0x0400 030f     Ethernet Controller
0x0400 0000 – 0x0400 02ff     Reserved by the Ethernet Controller

0x00FE 0000 - 0x00FF FFFF     128 kBytes reserved flash area (FIS directory)
0x00FC 0000 - 0x00FD FFFF     128 kBytes reserved flash area (RedBoot config)
0x0004 0000 - 0x00FB FFFF     15,5 MBytes flash area available
0x0000 0000 - 0x0003 FFFF     256 kBytes reserved flash area (RedBoot)
```

Note

The flash memory has an erase block size of 128 kBytes.

Interrupts

The following PXA255 GPIO pins are internally used on the TRITO-LP module for interrupts:

GPIO number	Device	active edge
2	Real Time Clock	Falling
3	Touch Panel Controller	Falling
4	Ethernet Controller	Rising

Internally used GPIO pins

The following PXA255 GPIO pins are internally used on the TRITON-LP module:

GPIO number	direction	used for ...
5	I/O	Control / data port for DS2430A silicon serial number
6	Output	power supply enable for RTC and DS2430A (**L:OFF**, H:ON)
7	Output	sleep control for Ethernet controller (L:Sleep, **H:Active**)
8	Output	I²C clock pin for real time clock
9	I/O	I²C data pin for real time clock
13	Output	I²C clock pin for core voltage DAC
14	I/O	I²C data pin for core voltage DAC