TX27

System On Module

- Processor Freescale i.MX27, 400 MHz
- RAM 64/128 MB mobile DDR-SDRAM
- ROM 128MB NAND Flash
- RTC DS1339 Real Time Clock
- Power supply Single 3.1V to 5.5V
- Size 26mm SO-DIMM
- Temp.-Range -20°C..85°C

Key Features

- 10/100Mbps Ethernet
- High Speed USB 2.0 OTG
- High Speed USB 2.0 Host
- LCD controller up to 800 x 600, 18bpp
- MPEG-4 H.263/H.264 Hardware Codec
- Camera Interface
- Several interfaces:
  6x UART, 2x SDIO, 2x SSI/AC97/I2S,
  I2C, CSPI, Keypad, Compact Flash

OS Support

- Windows Embedded CE
- Linux 2.6
- RedBoot Bootloader

Development System

- Starter-Kit V

400 MHz ARM9

freescale™ semiconductor

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Board highlights:

- world's smallest i.MX computer on module
- standard TX-DIMM pinout
- low power consumption
- easy to use
- low cost

The TX27 is the first member of a module series, specially designed for Freescales i.MX multimedia processors. TX modules are complete computers, implemented on a board smaller than a credit card, and ready to be designed into your embedded system. TX modules includes a Freescale® i.MX processor, SDRAM and Flash memory. The integrated LCD-controller enables direct connection of an LCD screen, and the standard PCMCIA interface permits simple extension and integration into a target system. The TX27 is specifically targeted at embedded applications where size, high cpu-performance and low power consumption are critical factors.

System on module

- Freescale® i.MX27, 400 MHz
- 64/128 MByte mobile DDR-SDRAM (32bit)
- 128 MByte NAND Flash memory
- DS1339 Real Time Clock
- DIMM200-module (67,6mm x 26 mm x 4,2mm)
- Operating temperature range -20°C..85°C

i.MX27

Derived from the popular i.MX21 processor, the i.MX27 processor adds an h.264 D1 hardware codec for high-resolution video processing, an Ethernet 10/100 MAC, security, plug-and-play connectivity and more power management features.

CPU

- ARM926EJ-S 400 MHz core
- 16 KB L1 I-Cache and D-Cache
- 16-channel DMA
- Smart Speed switch

Standard TX-DIMM interface
Universal 1.8V Interfaces:

- 4-wire UART (x3)
- up to 24-bit LCD Interface (depending on processor type)
- Camera IF
- I2C
- SSI/AC97/I2S (x2)
- 16-bit Compact Flash & Memory Interface
- 4-wire SDIO (x2)
- Keypad 5x5
- CSPI

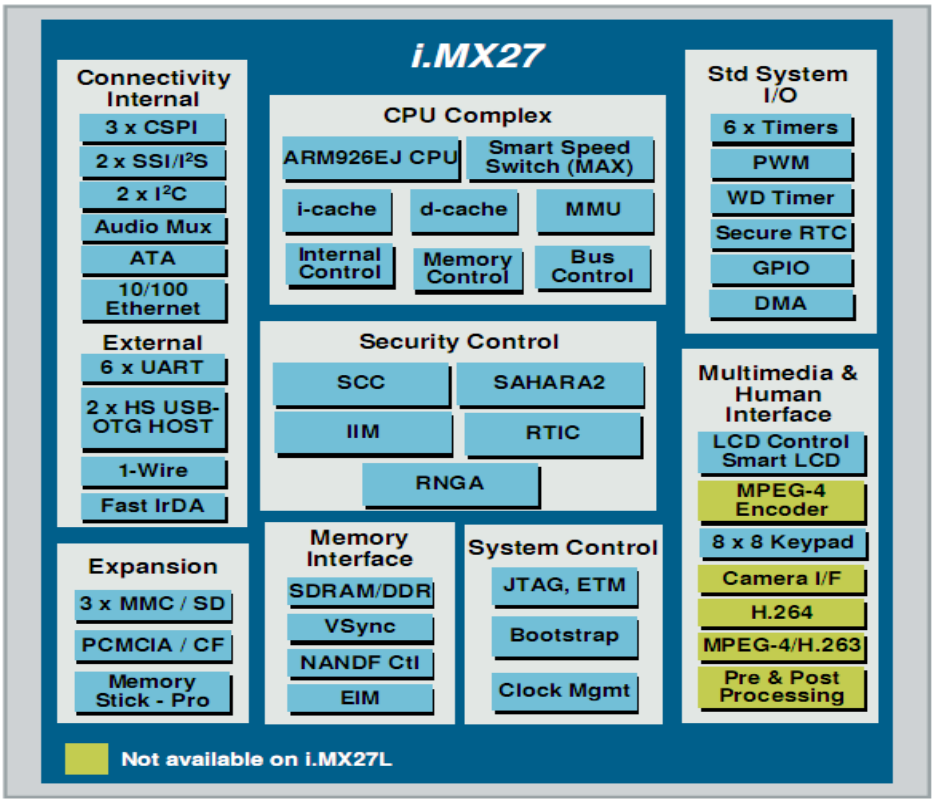
High-Speed communication interfaces incl. onboard PHY allows direct use of connectors/magnetics on the baseboard without the need for additional logic:

- 10/100 Mbps Ethernet
- High Speed USB 2.0 OTG
- High Speed USB 2.0 Host

Power Supply
The TX27 accepts an input voltage from various sources:

- 1-cell Li-Ion/Polymer (3.1V to 4.2V)
- 5.0V USB supply or AC wall adapter
- 3.3V

Up to 1A output current 1.8V and 3.3V power supply outputs of the TX27 can also be used on the baseboard.



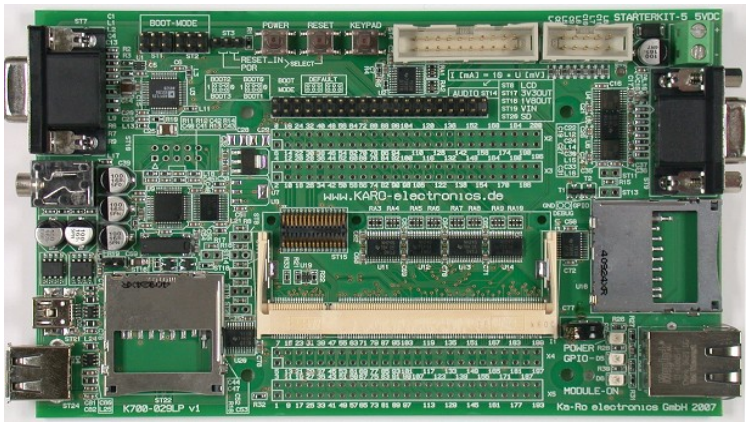
Ordering Information

Order Number	i.MX27	SDRAM	Flash	Temp.
TX27/400/64S/128/E85	400MHz	64MB	128MB	-20°C..85°C
TX27/400/128S/128/E85	400MHz	128MB	128MB	-20°C..85°C

2010-11-04

STARTER-KIT V

The Starter-Kit V is a ready-to-use development system for building applications based on the TX embedded processor boards.



- DIMM200 TX socket
- Two SD-card sockets
- USB 2.0 OTG and USB 2.0 Host connector
- D-SUB 15 VGA connector
- 40pin LCD flat cable header
- 3.5mm headphone connector
- JTAG interface
- SGTL5000 audio codec
- TSC2007 touchscreen controller
- RS232 on 10pin flat cable and SUB-D header
- All pins of the TX socket are connected to daughter board slot for easy application design-in
- 10/100 Mbit/s Ethernet
- 5VDC Power Supply by USB-OTG or power jack.
- 100mm x 160mm
- Schematics of the base board are included for reference.

DISPLAY OPTION

The optional display comes with an FFC cable and a small adapter PCB which can be plugged directly onto the Starter-Kit 40pin LCD header.

- 5,7 inch TFT display
- 640 x 480 dots
- White LED backlight
- Touchsceen

PINOUT

PIN	Type	TX-STANDARD	i.MX27 Signal/Pad Name	Alternate	GPIO	Description
POWER SUPPLY						
1-4	power	VIN	-			Module power supply input (3.0V-5.5V)
5-7	power	1V8_OUT	-			1.8V buck regulator output, up to 1A
8	1V8	BOOTMODE			47K-PU	Boot mode select H: Boot from NAND / L: Boot from UART/USB
9-12	power	3V3_OUT	-			3.3V buck regulator output, up to 1A
13	power	VBACKUP	-			DS1339 RTC backup power supply. Supply voltage must be held between 1.3V and 3.7V for proper RTC operation. This pin can be connected to a primary cell such as a lithium button cell. Additionally, this pin can be connected to a rechargeable cell or a super cap when used with the trickle charge feature.
Reset						
14	2.8V to 5.5V	PMIC_PWR_ON	-		PB24 47K-PD	This is an active high push button input which can be used to signal PWR_ON and PWR_OFF events to the CPU by controlling the PMIC ext_wakup signal and select contents of PMIC register 8H'88. Connected to a GPIO.
15	1V8	#RESET_OUT	#RESET_OUT			Reset Output - active low output: can be caused by all reset source: power on reset, system reset (RESET_IN), and watchdog reset.
16	2V8	#PMIC_RESET_IN	-		~14K-PU	Power On Reset—Active low input signal. Typically a push button reset or driven by an open collector output. This signal is also driven low by BATT_FLT. Please refer to the PMIC datasheet for details. Leave unconnected, if not used.
17	1V8	#RESET_IN	#RESET_IN			Master Reset—External active low Schmitt trigger input signal. When this signal goes active, all modules (except the reset module, SDRAMC module, and the clock control module) are reset.
Ethernet						
19	analog	ETN_TXN	-			Transmit Data Negative: 100Base-TX or 10Base-T differential transmit output to magnetics.
20	1V8	#ETN_LINKLED	-			Active low LINK ON indication: Active indicates that the link is on.
21	analog	ETN_TXP	-			Transmit Data Positive: 100Base-TX or 10Base-T differential transmit output to magnetics.
22	power	ETN_3V3	-			+3.3V analog power supply output to magnetics
23	analog	ETN_RXN	-			Receive Data Negative: 100Base-TX or 10Base-T differential receive input from magnetics.
24	1V8	#ETN_ACTLED	-			Active low ACTIVITY indication: Active indicates that there is Carrier sense (CRS) from the active PMD.
25	analog	ETN_RXP	-			Receive Data Positive: 100Base-TX or 10Base-T differential receive input from magnetics.
26	GND	GND	-			
USB-HOST						
27	3V3	USBH_VBUSEN	-			Active high external 5V supply enable. This pin is used to enable the external VBUS power supply.
28	3V3	#USBH_OC	USBH1_RXDP	UART4_RXD	PB31 47K-PU	Active low over-current indicator input connected to a GPIO. This signal can be used as an input only.
29	analog	USBH_DM	-			D- pin of the USB cable
30	analog	USBH_VBUS	-			VBUS pin of the USB cable. This pin is used for the VBUS comparator inputs.
31	analog	USBH_DP	-			D+ pin of the USB cable
32	GND	GND	-			
USB-OTG						
33	3V3	USBOTG_ID	-			ID pin of the USB cable. For an A-Device ID is grounded. For a B-Device ID is floated.
34	3V3	USBOTG_VBUSEN	-			Active high external 5V supply enable. This pin is used to enable the external VBUS power supply.
35	analog	USBOTG_DM	-			D- pin of the USB cable
36	3V3	#USBOTG_OC	USBH1_TXDP	UART4_CTS	PB29 47K-PU	Active low over-current indicator input connected to a GPIO. This signal can be used as an input only.
37	analog	USBOTG_DP	-			D+ pin of the USB cable
38	analog	USBOTG_VBUS	-			VBUS pin of the USB cable. This pin is used for the VBUS comparator inputs.
39	GND	GND	-			

PIN	Type	TX-STANDARD	i.MX27 Signal/Pad Name	Alternate	GPIO	Description
I2C						
40	1V8	I2C_DATA	I2C_DATA		PD17	I2C Data
41	1V8	I2C_CLK	I2C_CLK		PD18	I2C Clock
PWM						
42	1V8	PWM	PWMO	TOUT2 TOUT3	PE5	PWM Output. This signal is multiplexed with PC_SPKOUT of PCMCIA, as well as TOUT2 and TOUT3 of the General Purpose Timer module
1-WIRE						
43	1V8	OWIRE	RTCK		PE16	JTAG Return Clock used to enhance stability of JTAG debug interface devices. This signal is multiplexed with 1-Wire; thus, utilizing 1-Wire will render RTCK unusable and vice versa
CSPI – Configurable Serial Peripheral Interface						
44	1V8	CSPI_SS0	CSPI1_SS0		PD28	Slave Select (Selectable polarity) signal
45	1V8	CSPI_SS1	CSPI1_SS1	EXT_DMAGRANT	PD27	Slave Select (Selectable polarity) signal, multiplexed with EXT_DMAGRANT
46	1V8	CSPI_MOSI	CSPI1_MOSI		PD31	Master Out/Slave In signal
47	1V8	CSPI_MISO	CSPI1_MISO		PD30	Master In/Slave Out signal
48	1V8	CSPI_SCLK	CSPI1_SCLK		PD29	Serial Clock signal
49	1V8	CSPI_RDY	CSPI1_RDY	EXT_DMAREQ_B	PD25	Serial Data Ready signal, shared with Ext_DMAReq_B signal
50	GND	GND				
SD – Secure Digital Interface 1						
51	1V8	SD1_CD	SSI1_RXD		PC21	SD Card Detect – connected to a GPIO
52	1V8	SD1_D[0]	SD1_D[0]	CSPI3_MISO	PE18	SD Data bidirectional signals—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 50 K–69 K external pull up resistor must be added.
53	1V8	SD1_D[1]	SD1_D[1]		PE19	
54	1V8	SD1_D[2]	SD1_D[2]		PE20	
55	1V8	SD1_D[3]	SD1_D[3]	CSPI3_SS	PE21	
56	1V8	SD1_CMD	SD1_CMD	CSPI3_MOSI	PE22	SD Command bidirectional signal—If the system designer does not want to make use of the internal pull-up, via the Pull-up enable register, a 4. 7K–69 K external pull up resistor must be added.
57	1V8	SD1_CLK	SD1_CLK	CSPI3_SCLK	PE23	SD Output Clock.
58	GND	GND				
UART1						
59	1V8	UART1_TXD	UART1_TXD		PE12	Transmit Data output signal
60	1V8	UART1_RXD	UART1_RXD		PE13	Receive Data input signal
61	1V8	UART1_RTS	UART1_RTS		PE15	Request to Send input signal
62	1V8	UART1_CTS	UART1_CTS		PE14	Clear to Send output signal
UART2						
63	1V8	UART2_TXD	UART2_TXD	KP_COL6	PE6	Transmit Data output signal
64	1V8	UART2_RXD	UART2_RXD	KP_ROW6	PE7	Receive Data input signal
65	1V8	UART2_RTS	UART2_RTS	KP_ROW7	PE4	Request to Send input signal
66	1V8	UART2_CTS	UART2_CTS	KP_COL7	PE3	Clear to Send output signal
UART3						
67	1V8	UART3_TXD	UART3_TXD		PE8	Transmit Data output signal
68	1V8	UART3_RXD	UART3_RXD		PE9	Receive Data input signal

PIN	Type	TX-STANDARD	i.MX27 Signal/Pad Name	Alternate	GPIO	Description
69	1V8	UART3_RTS	UART3_RTS		PE11	Request to Send input signal
70	1V8	UART3_CTS	UART3_CTS		PE10	Clear to Send output signal
71	GND	GND				
KEYPAD						
72	1V8	KP_COL[0]	KP_COL[0]			Keypad Column selection signals.
73	1V8	KP_COL[1]	KP_COL[1]			
74	1V8	KP_COL[2]	KP_COL[2]			
75	1V8	KP_COL[3]	KP_COL[3]			
76	1V8	KP_COL[4]	KP_COL[4]			
77	1V8	KP_ROW[0]	KP_ROW[0]			Keypad Row selection signals.
78	1V8	KP_ROW[1]	KP_ROW[1]			
79	1V8	KP_ROW[2]	KP_ROW[2]			
80	1V8	KP_ROW[3]	KP_ROW[3]			
81	1V8	KP_ROW[4]	KP_ROW[4]			
82	GND	GND				
SSI - Serial Audio Port (Configurable to I2S Protocol and AC97)						
83	1V8	SSI3_INT	SSI1_CLK		PC23	GPIO
84	1V8	SSI3_RXD	SSI3_RXD	SLCDC2_RS	PC29	Receive serial data
85	1V8	SSI3_TXD	SSI3_TXD	SLCDC2_CS	PC30	Transmit serial data
86	1V8	SSI3_CLK	SSI3_CLK	SLCDC2_CLK	PC31	Serial clock
87	1V8	SSI3_FS	SSI3_FS	SLCDC2_D0	PC28	Frame Sync
88	GND	GND				
SSI - Serial Audio Port (Configurable to I2S Protocol and AC97)						
89	1V8	SSI4_INT	SSI1_FS		PC20	GPIO
90	1V8	SSI4_RXD	SSI4_RXD		PC17	Receive serial data
91	1V8	SSI4_TXD	SSI4_TXD		PC18	Transmit serial data
92	1V8	SSI4_CLK	SSI4_CLK		PC19	Serial clock
93	1V8	SSI4_FS	SSI4_FS		PC16	Frame Sync
94	GND	GND				
Secure Digital Interface 2						
95	1V8	SD2_CD	SSI1_TXD		PC22	SD Card Detect - connected to a GPIO
96	1V8	SD2_D[0]	SD2_D[0]	MSHC_DATA0	PB4	SD Data bidirectional signals.
97	1V8	SD2_D[1]	SD2_D[1]	MSHC_DATA1 SLCDC1_CLK	PB5	
98	1V8	SD2_D[2]	SD2_D[2]	MSHC_DATA2 SLDCD1_D0	PB6	
99	1V8	SD2_D[3]	SD2_D[3]	MSHC_DATA3 SLCDC1_RS	PB7	
100	1V8	SD2_CMD	SD2_CMD	MSHC_BS SLCDC1_CS	PB8	SD Command bidirectional signal.
101	1V8	SD2_CLK	SD2_CLK	MSHC_SCLK	PB9	SD Output Clock signal.
102	GND	GND				
CMOS Sensor Interface						

PIN	Type	TX-STANDARD	i.MX27 Signal/Pad Name	Alternate	GPIO	Description
103	1V8	CSI_D0	CSI_D0	UART6_TXD	PB10	Sensor port data
104	1V8	CSI_D1	CSI_D1	UART6_RXD	PB11	Sensor port data
105	1V8	CSI_D2	CSI_D2	UART6_CTS	PB12	Sensor port data
106	1V8	CSI_D3	CSI_D3	UART6_RTS	PB13	Sensor port data
107	1V8	CSI_D4	CSI_D4		PB14	Sensor port data
108	1V8	CSI_D5	CSI_D5		PB17	Sensor port data
109	1V8	CSI_D6	CSI_D6	UART5_TXD	PB18	Sensor port data
110	1V8	CSI_D7	CSI_D7	UART5_RXD	PB19	Sensor port data
111	GND	GND				
112	1V8	CSI_HSYNC	CSI_HSYNC	UART5_RTS	PB21	Sensor port horizontal sync
113	1V8	CSI_VSYNC	CSI_VSYNC	UART5_CTS	PB20	Sensor port vertical sync
114	1V8	CSI_PIXCLK	CSI_PIXCLK		PB16	Sensor port data latch clock
115	1V8	CSI_MCLK	CSI_MCLK		PB15	Sensor port master clock
116	GND	GND				
LCD Controller and Smart LCD Controller						
117	1V8	LD [0]	USBH1_TXDM	UART4_TXD SLCDC1_DAT3	PB28	GPIO (output only)
118	1V8	LD [1]	CONTRAST		PA30	This signal is used to control the LCD bias voltage as contrast control
119	1V8	LD [2]	LD [0]	SLCDC1_DAT0	PA6	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.
120	1V8	LD [3]	LD [1]	SLCDC1_DAT1	PA7	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.
121	1V8	LD [4]	LD [2]	SLCDC1_DAT2	PA8	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.
122	1V8	LD [5]	LD [3]	SLCDC1_DAT3	PA9	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.
123	1V8	LD [6]	LD [4]	SLCDC1_DAT4	PA10	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.
124	1V8	LD [7]	LD [5]	SLCDC1_DAT5	PA11	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.
125	1V8	LD [8]	CLS	SLCDC1_RS	PA25	Start signal output for gate driver. This signal is invert version of PS (Sharp panel dedicated signal).
126	1V8	LD [9]	PS	SLCDC1_CS	PA26	Control signal output for source driver (Sharp panel dedicated signal).
127	1V8	LD [10]	LD [6]	SLCDC1_DAT6	PA12	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.
128	1V8	LD [11]	LD [7]	SLCDC1_DAT7	PA13	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.
LCD Controller and Smart LCD Controller						
129	GND	GND				
130	1V8	LD [12]	LD [8]	SLCDC1_DAT8	PA14	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.
131	1V8	LD [13]	LD [9]	SLCDC1_DAT9	PA15	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.
132	1V8	LD [14]	LD [10]	SLCDC1_DAT10 SLCDC1_DAT2	PA16	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.
133	1V8	LD [15]	LD [11]	SLCDC1_DAT11 SLCDC1_DAT3	PA17	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.
134	1V8	LD [16]	REV	SLDCD1_D0	PA24	Signal for common electrode driving signal preparation (Sharp panel dedicated signal).
135	1V8	LD [17]	SPL_SPR	SLCDC1_CLK	PA27	Sampling start signal for left and right scanning.
136	1V8	LD [18]	LD [12]	SLCDC1_DAT12 SLCDC1_DAT4	PA18	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.
137	1V8	LD [19]	LD [13]	SLCDC1_DAT13 SLCDC1_DAT5	PA19	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.
138	1V8	LD [20]	LD [14]	SLCDC1_DAT14 SLCDC1_DAT6	PA20	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.
139	1V8	LD [21]	LD [15]	SLCDC1_DAT15 SLCDC1_DAT7	PA21	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.

PIN	Type	TX-STANDARD	i.MX27 Signal/Pad Name	Alternate	GPIO	Description
140	1V8	LD [22]	LD [16]	Ext_DMAGrant_B	PA22	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.
141	1V8	LD [23]	LD [17]		PA23	LCD Data Bus—All LCD signals are driven low after reset and when LCD is off.
142	GND	GND				
143	1V8	HSYNC			PA28	Line Pulse or HSync
144	1V8	VSYNC			PA29	Frame Sync or Vsync—This signal also serves as the clock signal output for gate; driver (dedicated signal SPS for Sharp panel HR-TFT)
145	1V8	OE_ACD			PA31	Alternate Crystal Direction/Output Enable
146	1V8	LSCLK			PA5	Shift Clock
147	GND	GND				
External Bus/Chip Select (EMI)						
148	1V8	PC_PWRON	PC_PWRON		PF16	PCMCIA signal, multiplexed with ATA ATA_DA2 signal; PF16
149	1V8	PC_CD1_B	PC_CD1_B		PF20	PCMCIA card detect signal, multiplexed with ATA ATA_DIOR signal; PF20
150	1V8	PC_BVD1	PC_BVD1		PF12	PCMCIA Battery voltage detect signal, multiplexed with ATA ATA_DMARQ signal; PF12
151	1V8	PC_BVD2	PC_BVD2		PF11	PCMCIA Battery voltage detect signal, multiplexed with ATA ATA_DMACK signalPF11
152	1V8	PC_VS1	PC_VS1		PF14	PCMCIA voltage sense signal, multiplexed with ATA ATA_DA1 signal; PF14
153	1V8	PC_VS2	PC_VS2		PF13	PCMCIA voltage sense signal, multiplexed with ATA ATA_DA0 signal; PF13
154	1V8	IOIS16	IOIS16		PF9	PCMCIA mode signal, multiplexed with ATA ATA_INTRQ signal; PF9
155	1V8	PC_RW_B	PC_RW_B		PF8	PCMCIA read write signal, multiplexed with ATA ATA_IORDY signal; PF8
156	1V8	PC_RST	PC_RST		PF10	PCMCIA card reset signal, multiplexed with ATA ATA_RESET_B signal; PF10
157	1V8	PC_WAIT_B	PC_WAIT_B		PF18	PCMCIA WAIT signal, multiplexed with ATA ATA_CS1 signal; PF18
158	1V8	PC_READY	PC_READY		PF17	PCMCIA READY/IRQ signal, multiplexed with ATA ATA_CS0 signal; PF17
159	1V8	PC_POE	PC_POE		PF7	PCMCIA output enable signal, multiplexed with ATA ATA_BUFFER_EN signal; PF7
160	GND	GND				
161	1V8	CS [0]	CS [0]			Chip Select
162	1V8	CS [1]	CS [1]			
163	1V8	CS [4]	CS [4]	CS5_DTACK	PF21	
164	1V8	ECB	ECB			Active low input signal sent by flash device to the EIM whenever the flash device must terminate an on-going burst sequence and initiate a new (long first access) burst sequence.
External Bus/Chip Select (EMI)						
165	1V8	EB0	EB0			Active low external enable byte signal that controls D [15:8], shared with PCMCIA PC_REG.
166	1V8	EB1	EB1			Active low external enable byte signal that controls D [7:0], shared with PCMCIA PC_IORD.
167	1V8	OE	OE			Memory Output Enable—Active low output enables external data bus, shared with PCMCIA PC_IOWR.
168	1V8	LBA	LBA			Active low signal sent by flash device causing external burst device to latch the starting burst address.
169	1V8	RW	RW			RW signal—Indicates whether external access is a read (high) or write (low) cycle. This signal is also shared with the PCMCIA PC_WE.
170	1V8	BCLK	BCLK			Clock signal sent to external synchronous memories (such as burst flash) during burst mode.
171	GND	GND				
172	1V8	A [0]	A [0]			Address bus signals
173	1V8	A [1]	A [1]			
174	1V8	A [2]	A [2]			
175	1V8	A [3]	A [3]			
176	1V8	A [4]	A [4]			

PIN	Type	TX-STANDARD	i.MX27 Signal/Pad Name	Alternate	GPIO	Description
177	1V8	A [5]	A [5]			
178	1V8	A [6]	A [6]			
179	1V8	A [7]	A [7]			
180	1V8	A [8]	A [8]			
181	1V8	A [9]	A [9]			
182	1V8	A [10]	A [10]			
183	GND	GND				
184	1V8	D[0]	D[0]			Data Bus signals
185	1V8	D[1]	D[1]			
186	1V8	D[2]	D[2]			
187	1V8	D[3]	D[3]			
188	1V8	D[4]	D[4]			
189	1V8	D[5]	D[5]			
190	1V8	D[**7**]	D[**7**]			Be aware! D[7] and D[6] are out of order!
191	1V8	D[**6**]	D[**6**]			Be aware! D[7] and D[6] are out of order!
192	1V8	D[8]	D[8]			
193	1V8	D[9]	D[9]			
194	1V8	D[10]	D[10]			
195	1V8	D[11]	D[11]			
196	1V8	D[12]	D[12]			
197	1V8	D[13]	D[13]			
198	1V8	D[14]	D[14]			
199	1V8	D[15]	D[15]			
200	GND	GND	GND			