TRACE32®

DEBUGGER, REAL-TIME TRACE, LOGIC ANALYZER

LEADING through Technology

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LAUTERBACH
DEVELOPMENT TOOLS

The **Company**

Lauterbach was founded in 1979 by Lothar Lauterbach. Three years later, his brother Stephan joined the team. Since then, the company has been managed by the two brothers.

The company now has over **30 years experience** in the field of development tools and embedded designs.

Lauterbach is a completely independent and privately owned company with steadfast connections to all key semiconductor manufacturers. This, combined with **ground-breaking innovations** and a genuine **focus on customer satisfaction**, has rewarded Lauterbach with exceptional growth throughout much of the company's history.

ADVANTAGES

Over 30 Years Experience

- High technology company
- Creative, competent, customer-focused
- Long-standing relationships with customers and partners
- Free of charge expert support

Global And Independent

- Headquarters in Germany, branch offices in China, France, Italy, Japan, UK and US
- Independent, privately owned company

THE HIGHEST LEVELS OF TECHNOLOGY AND QUALITY

All software and hardware development is carried out at the company headquarters in Höhenkirchen-Siegertsbrunn, near Munich. 80% of the work-force is comprised of software or hardware engineers.

Incorporating the latest methods of development, Lauterbach puts great emphasis on creating state-of-the-art development tools. The **outstanding quality and stability** of both the hardware and software are well known and appreciated by the worldwide embedded developer community.

TIME TO MARKET

The concept of **time to market,** which is crucial for developments by Lauterbach customers, is even more relevant for Lauterbach itself. When customers want to start developing with the very latest generations of microprocessors, they can rely on Lauterbach for being the first to market these tools. Thanks to the high level of cooperation and exchange of information between Lauterbach and the industry's leading semiconductor manufacturers, time and again, Lauterbach has proven this concept.

LOTHAR LAUTERBACH
Managing Director (commercial)

STEPHAN LAUTERBACH
Managing Director (technical)

WORLDWIDE MARKET LEADER FOR DEBUG TOOLS

Lauterbach, already established as a technology leader, evolved into the worldwide market leader and supplier of microprocessor development tools. By the end of 2008, more than **80,000 development seats** across the globe have been equipped with Lauterbach debugger tools and assisting an even larger number of developers. In the embedded systems market, no other debugging tool spans such a broad user community.

The company has its own branch offices in the most market bearing regions of the world. In the United States, it has offices on both the east and west coast. Europe is complimented by offices in the UK, France and Italy. Asia is represented by offices in China and Japan. In all other countries Lauterbach has long standing agreements with technically competent partners, guaranteeing global supply and support for the entire range of Lauterbach products.

A LONG TERM INVESTMENT

The decision to make Lauterbach systems modular and to provide an open interface has meant that customers can protect their investment and help guard against obsolescence. The first generation TRACE32 systems have been compatible with follow up designs for over 15 years. The tools are easily scalable. Initial tools can be purchased to satisfy an immediate need, with the option to buy additional modules later, expanding the tool's capabilities.

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LAUTERBACH
DEVELOPMENT TOOLS

PD = PowerDebug
PT = PowerTrace
PI = PowerIntegrator
PP = PowerProbe
IDE = PowerView

The *Tool Chain*

Lauterbach provides integrated debug environments for embedded designs.

The tool chain includes:

- **Debugger**
- **Real-time trace for program/data flow**
- **Logic analyzer**

These capabilities are implemented by dedicated hardware components.

The common user interface PowerView and a joint system bus provide a seamless integration of all the tools into the debug environment.

PowerDebug

A debug system comprises the universal debugger hardware **PowerDebug** and a **debug cable** specific to the processor architecture.

ADVANTAGES

Integrated Debug Environment Including

- Debugger
- Real-time trace for program/data flow
- Logic analyzer for ports, bus protocols and communication interfaces

Universal Base Modules

All base modules are fully universal. The adaptation to a specific processor architecture is done by

- A debug cable to connect to the onchip debugging interface
- A preprocessor/NEXUS adapter to connect to the trace port
- Standard and application specific probes for the logic analyzer

Common IDE

- To control all devices in one GUI
- To display the debug and trace information in one GUI
- To show the logical/timing correlation between all displayed information

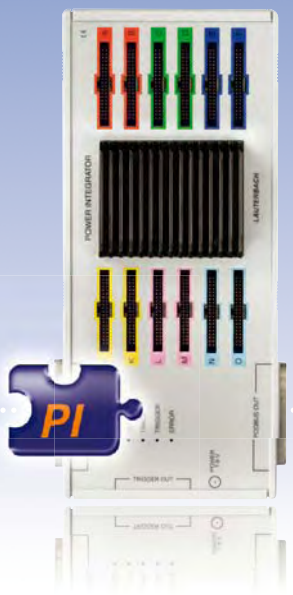
MODULAR AND UPGRADEABLE

All base modules are completely universal. Migration to a new processor architecture is very simple – just exchange the debug cable and the preprocessor/NEXUS adapter.

EFFORTLESS HIGH-SPEED ANALYSIS

The debug environment is designed to provide quick and efficient testing of your embedded design. Even complex analyses can be performed in a very short time.

- A fast host interface ensures an efficient download of the application program as well as a rapid upload of the trace information.
- System software which is optimized for high-speed devices guarantees very fast debugging and trace evaluation.



PowerTrace

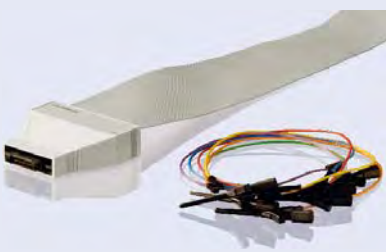
A real-time trace system to record program/data flow data and timing comprises the universal trace hardware **PowerTrace** and a **preprocessor/ NEXUS adapter** specific to the processor architecture.

PowerIntegrator

The logic analyzer with high speed clock rate consists of the universal analyzer hardware **PowerIntegrator** and standard/application specific **probes** for target connection.

PowerProbe

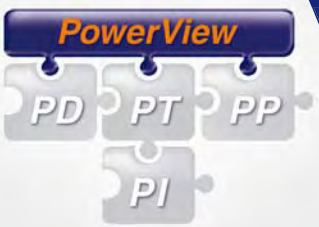
The **PowerProbe** is a logic analyzer with medium speed clock rate. Outstanding features are the integrated pattern generator and a **FPGA probe** to record condition changes on FPGA internal nodes.



CONFIGURATION

The debugger forms the heart of the system.
The other hardware modules can be added as needed to fulfill requirements specific to your project.

PowerView – A Universal Interface



PowerView provides an integrated debug environment and an universal interface for the entire tool family. Menus, toolbars and dialog boxes offer intuitive and fast access to all of the debug, real-time trace and logic analyzer features.

CONSISTENT CONTROL

PowerView guarantees a consistent look and feel for all tools within the integrated development environment.

- When the application program on the target processor is started or stopped via the debugger, the program/data flow trace and the logic analyzer can be synchronized so they start or stop simultaneously.
- To analyze complex or intermittent problems, trigger conditions can be programmed into all tools. A seamless cross-trigger system guarantees the accurate collection of software/hardware information and facilitates easy identification of the cause of error conditions.

COHERENT DISPLAY

All of the software and hardware information required for debugging, performance analysis and quality assurance of the overall embedded design is displayed in a common GUI.

- All tools can use a common symbol database.
- The time relationship between the program/data flow information and the signal recording of the logic analyzer can be viewed at a glance.
- The logical source code context for all of the trace/logic analyzer information is visible on a mouse click.

ADVANTAGES

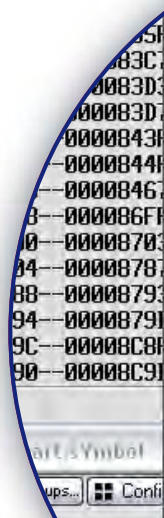
Uniform Look-And-Feel For All Architectures

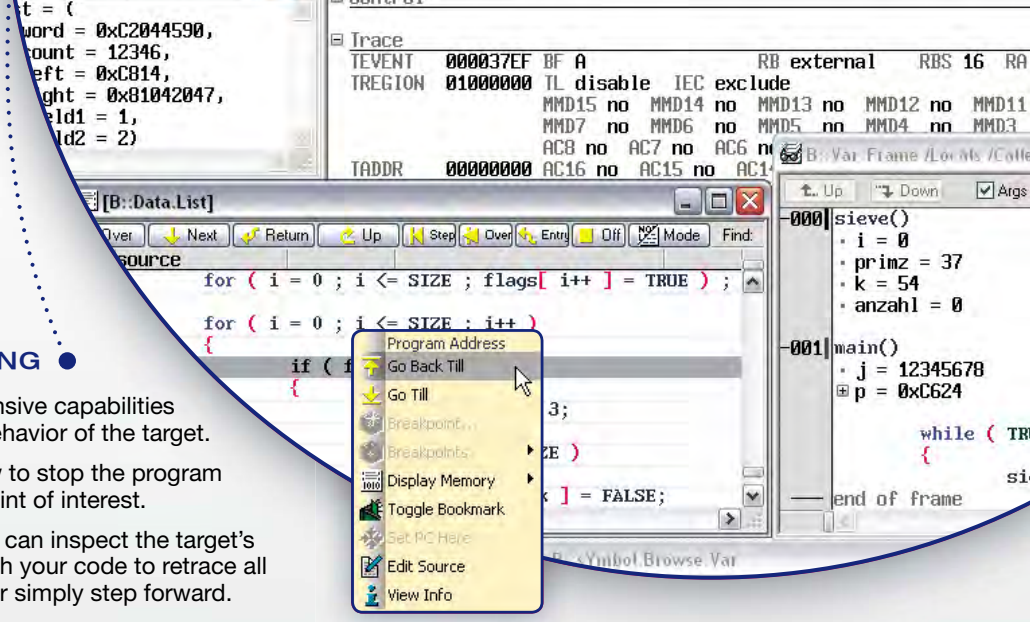
Customers who are familiar with PowerView find it easy to migrate to any other processor architecture; 98% of the IDE is common for all supported processor architectures.

Open System

The PowerView IDE is a flexible user interface that allows every developer to configure the environment to meet their specific needs. This includes:

- Free selection of the host interface and the host operating system
- Free selection of the programming language and the appropriate compiler
- Free selection of the RTOS
- Free selection of the CASE tool

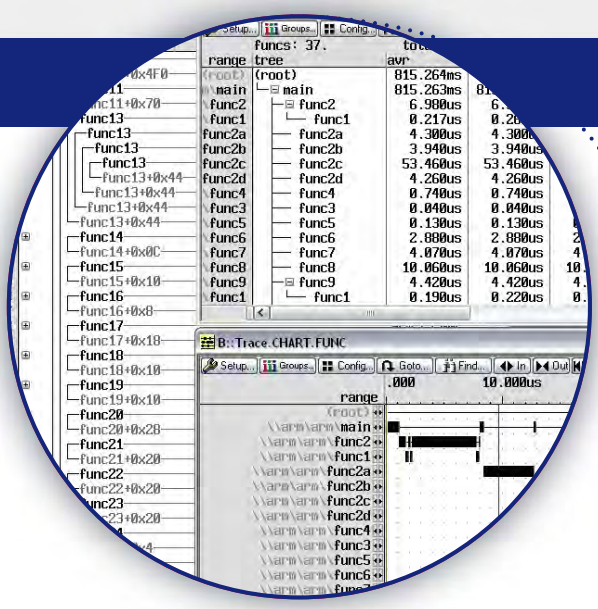




EFFECTIVE DEBUGGING

The debugger provides extensive capabilities to control and analyze the behavior of the target.

- Effective breakpoints allow to stop the program execution exactly at the point of interest.
- At the point of interest you can inspect the target's state, run backward through your code to retrace all executed program steps, or simply step forward.



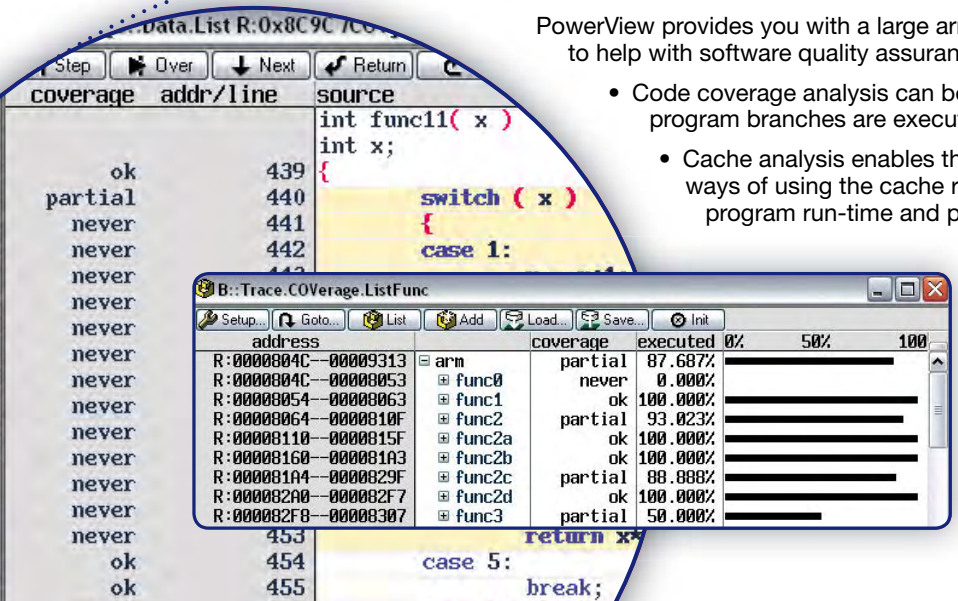
ANALYSIS OF THE SYSTEM PERFORMANCE

PowerView offers a vast number of options for evaluating the real-time characteristics of your embedded design. This includes the measurement of function run-times and analysis of the call tree. Graphical displays assist in the intuitive evaluation of your results.

QUALITY ASSURANCE

PowerView provides you with a large array of functions to help with software quality assurance. For example:

- Code coverage analysis can be used to ensure that all program branches are executed during the test phase.
- Cache analysis enables the user to explore more effective ways of using the cache resulting in systems with optimal program run-time and power consumption.



The *Adaptable* – *RTOS Debugger*

The standard PowerView debug environment includes a **configurable RTOS debugger** to provide the user with symbolic debugging capability in real-time operating systems. This interface is obtainable for all commonly available RTOS variants and is an integral part of PowerView. An API is provided to allow developers to use their own interface to any proprietary OS.

The RTOS debugger provides easy access to **task lists** and other kernel related information. It enables **effective debugging** of targets running an OS as well as extensive **run-time analysis.**

ADVANTAGES

Adaptive RTOS Debugger With

- Ready-to-run support for all common RTOS types
- API for proprietary RTOS

Sophisticated RTOS Debugging

- Real-time, non-intrusive display of OS system resources on supported hardware
- Task-related breakpoints
- Task stack coverage
- Task context display
- Full integrated MMU support
- Simultaneous debugging of several processes, drivers and the kernel
- Task performance measurement

DEBUG YOUR SOFTWARE FROM STARTUP

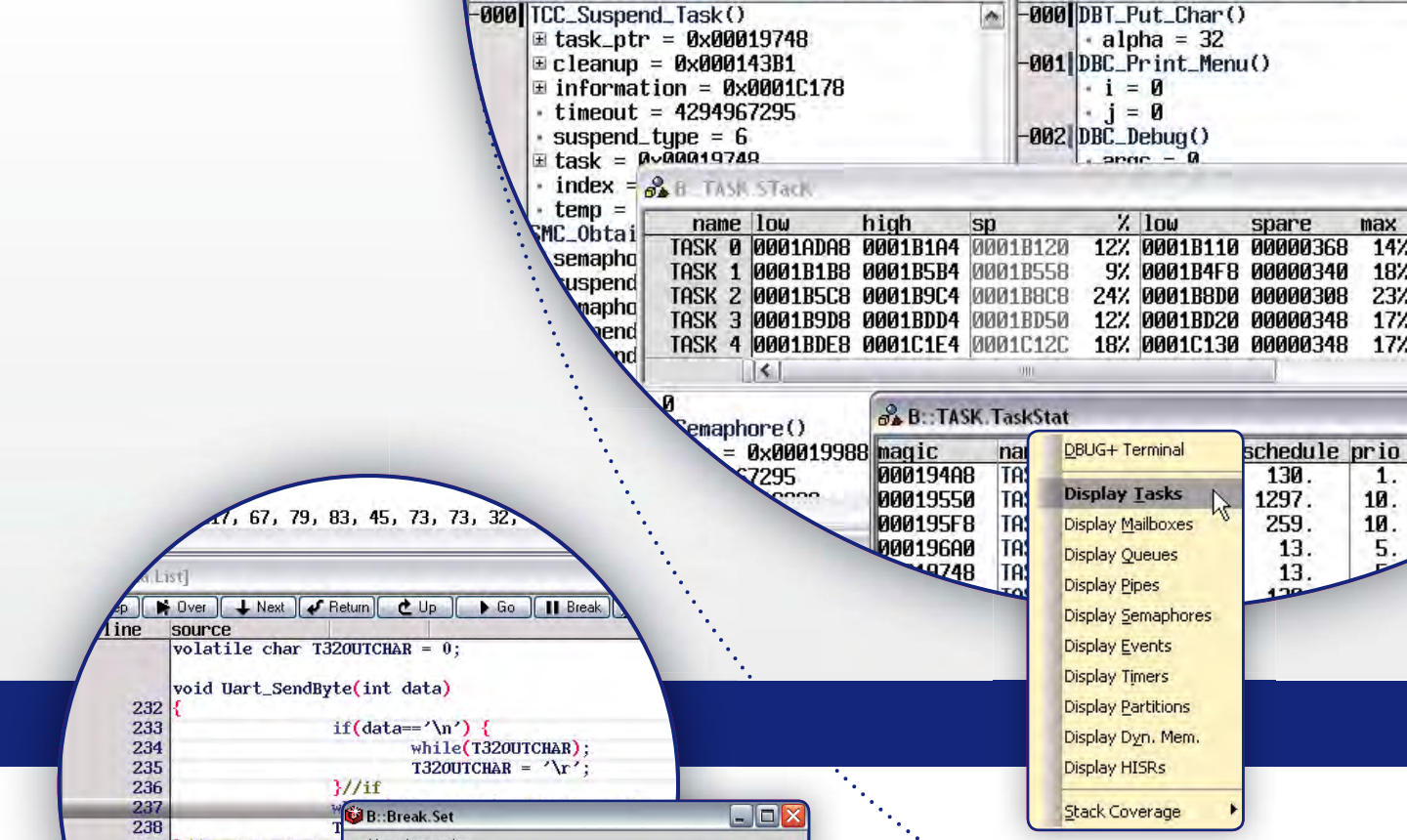
As debug information is provided by the onchip debug interface it becomes possible to **test and analyze every aspect** of the target/RTOS including the bootstrap code, the target initialization, the interrupts, the drivers and the kernel itself.

For RTOS types which **dynamically load processes**, a special detection mechanism is provided that catches the processor exactly on the entry point. This allows the developer to debug each process right from its start.

FULL MMU SUPPORT

The standard interface, PowerView, also provides the user with an advanced MMU support capability featuring full access to the target memory using either **virtual or physical addresses**. A transparent display of hardware and software/OS based translation tables is offered as well.

The MMU support allows the RTOS debugger to handle the use of **multiple address spaces**. Several processes that run at the same virtual address can be debugged simultaneously. The user has unrestricted abilities to monitor all process address spaces.

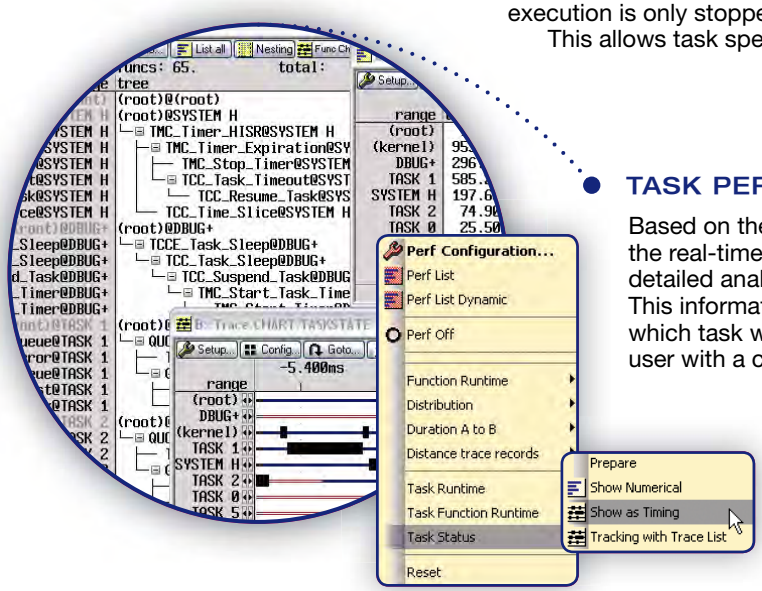


EASY ACCESS TO RTOS FEATURES

When the user activates the RTOS awareness included in the debugger, the GUI is automatically customized with the RTOS specific menu extensions. These extensions provide a fast and easy access to all the features of the RTOS debugger.

TASK SPECIFIC BREAKPOINTS

Breakpoints can be set task specific. This means the program execution is only stopped at a breakpoint if the specific task is active. This allows task specific debugging even in shared code.



TASK PERFORMANCE MEASUREMENT

Based on the program and data flow sampled by the real-time trace, the RTOS debugger can provide a detailed analysis of the task run-times and task switches. This information can then be displayed graphically, showing which task was active at a given time, thus providing the user with a clear view of the system behavior.

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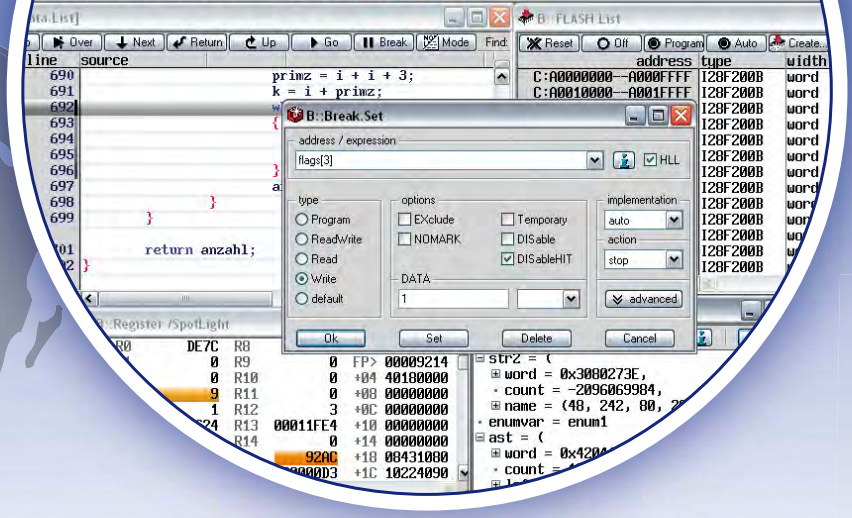


The **Debugger** – **PowerDebug**

PowerView PD PT PP PI

The debug system consists of the universal hardware module **PowerDebug** and the **debug cable** for the chosen processor architecture. As the PowerDebug is completely universal, migration to a new processor architecture is very simple – just exchange the debug cable.

APPLICATIONS

The main tasks of the debugger are:

- To download the user program to the target memory.
  This includes programming the processor internal and external FLASH.
- To start and stop the program execution on the target.
  Effective breakpoints help you to stop the program execution exactly at the point of interest.
- To inspect the processor and the overall target state.
  A concise and intuitive display assists the user in verifying correct functionality of the target system.

50+ PROCESSOR ARCHITECTURES

This debugger supports more than 50 processor architectures including RISC architectures, DSPs and FPGAs with embedded cores.

Thanks to the high level of cooperation and information exchange between Lauterbach and the industry's leading semiconductor manufacturers our debuggers are always the first to support new processor architectures.

MULTICORE/MULTIPROCESSOR DEBUGGING

The debugger provides an easy to configure environment supporting multicore/multiprocessor debug sessions for any mixture of RISC, DSP or IP cores. A synchronous start and stop of multiple cores/processors is fully supported.

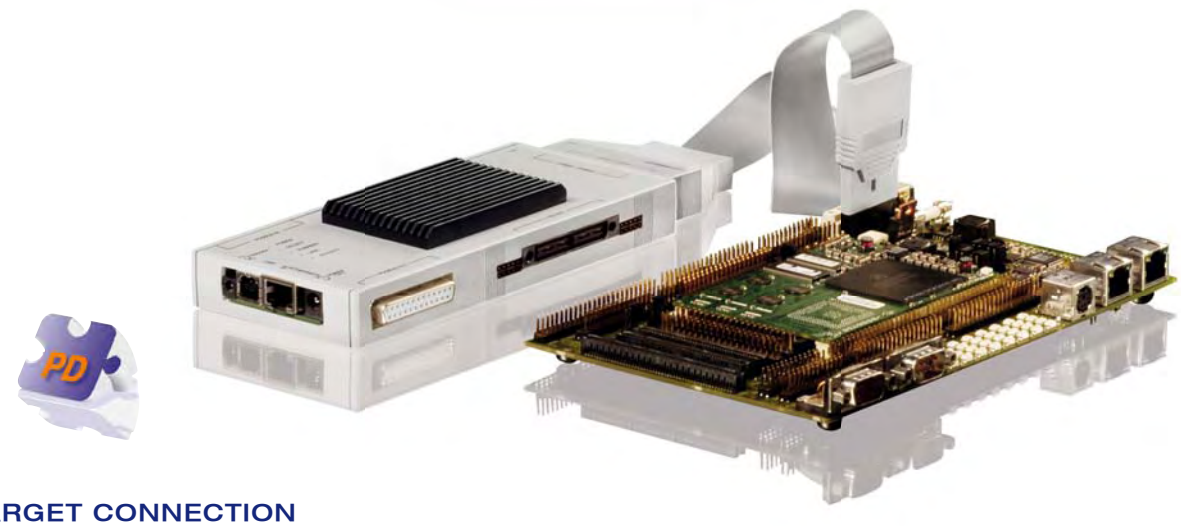
ADVANTAGES

Components

- Universal hardware module PowerDebug
- Architecture specific debug cable

Specification

- USB2.0, Gigabit ethernet interface to host
- PPC440 GX at 500 MHz as the system controller for high-speed debugging
- Optimized system software allows download speeds up to 5 MByte/s
- Fast system bus to connect the PowerTrace, the PowerIntegrator and the PowerProbe
- FPGA based firmware allows updates for new technologies



TARGET CONNECTION

The **debug cable** connects the debugger to the standard onchip debug connector as defined by the silicon manufacturer.

- Support is provided for voltage ranges from 0.4V to 5V.
- **Halfsize** adapters allow the designer to reduce the area required by the connector on the target system to only a quarter of the standard footprint.

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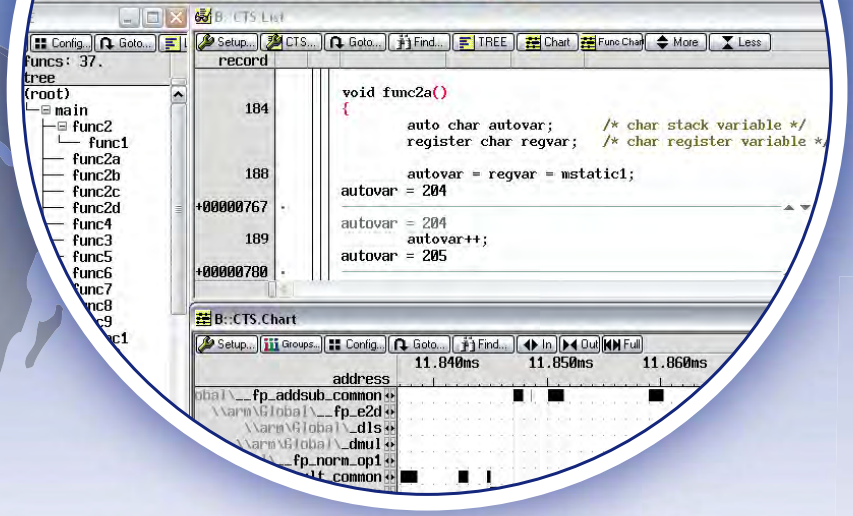

The **Real-Time Trace – PowerTrace**

The real-time trace consists of the universal hardware module **PowerTrace** and the **preprocessor/NEXUS adapter** for the chosen processor architecture. As the PowerTrace is completely universal, migration to a new processor architecture is very easy – simply exchange the preprocessor/NEXUS adapter.

APPLICATIONS

The main task of the real-time trace is to provide fast and systematic trouble shooting capabilities to detect complex errors that only occur under run-time conditions.
In addition the program/data flow recorded by the real-time trace is time-stamped, thus allowing an overall analysis of the system's performance. The huge amount of trace information that can be collected provides a basis for quality assurance features like code coverage or cache analysis.

30+ PROCESSOR ARCHITECTURES

A real-time trace is offered for more than 30 processor architectures. Over the last 7 years Lauterbach achieved world leading expertise for trace port protocols such as the Embedded Trace Macrocell for the ARM architecture or NEXUS (e.g. for the PowerPC architecture).

HIGH SPEED TRACE UPLOAD

PowerTrace and PowerDebug are designed for high-speed upload of up to 4 GigaByte of program and data flow information to the host system. Fast trace evaluation and analysis is guaranteed through advanced compression technologies and speed-optimized system software.

ADVANTAGES

Components

- Universal hardware module PowerTrace
- Architecture specific preprocessor/NEXUS adapter

Specification

- 1, 2 or 4 GigaByte trace memory
- Trace port speed in excess to 600 MHz parallel and 6.25 GBit serial
- 64 bit time stamp with 5 ns resolution
- Fast system bus to connect to PowerDebug for uploading the trace information via USB 2.0 or Gigabit ethernet interface
- Optimized system software permitting upload speeds of 100+ MByte/s
- 16 channels for arbitrary target signals
- FPGA based firmware allows updates for new technologies

TARGET CONNECTION

The **preprocessor/NEXUS adapter** connects the real-time trace to the standard trace port connector as defined by the silicon manufacturer.

- Flexible high-speed extension cables guarantee the best possible connection to the target.
- The preprocessor contains a self-calibrating hardware (AutoFocus) to ensure signal integrity.

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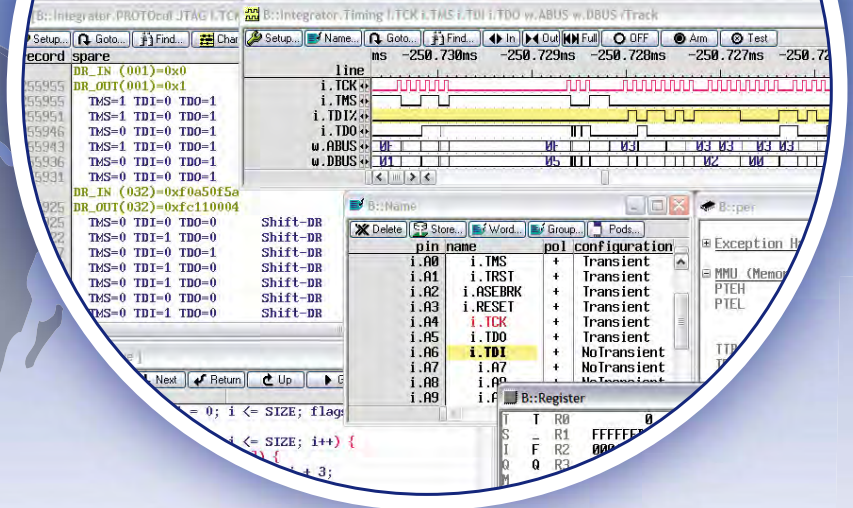


The **Logic Analyzer** – **PowerProbe/PowerIntegrator**

PowerView

PD PT PP PI

The logic analyzers consist of the universal hardware module **PowerIntegrator/PowerProbe** and standard/application specific **probes** for connection to the target.

APPLICATIONS

The main task of the logic analyzer is to record bus protocols, communication interfaces, interrupts and ports in order to analyze their timing. The common IDE PowerView provides ready-to-run software interfaces:

- To translate bus protocols into a program and data flow trace by using the common symbol database of the debugger.
- To perform various protocol analyses based on the raw data recorded for a communication interface.

FULL INTEGRATION

The logic analyzer is designed as integral part of the debug environment. This means consistent control and coherent display of all information through the common IDE PowerView. For instance the time relation between the program/data flow information sampled by the real-time trace and signals recorded by the logic analyzer can be viewed at a glance.

OPTIMIZED RECORDING

The logic analyzer supports timing, state and transient recording. Simple and complex filters allow an optimized utilization of the trace memory. To analyze complex timing correlation, trigger conditions can be programmed to stop either the logic analyzer recording or the program execution at the precise point of interest.

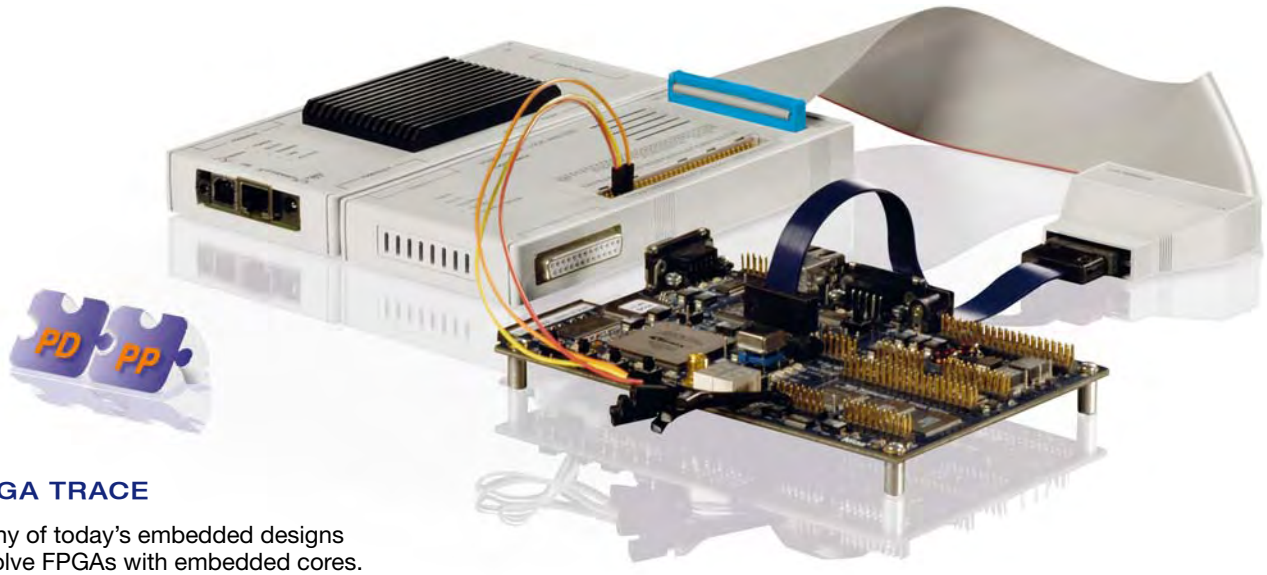
ADVANTAGES

PowerIntegrator

- 204 channels with 250 MHz timing mode (102 channels with 500 MHz)
- 204 channels with 200 MHz state mode (102 channels with 200 MHz double data rate)
- 16 data selectors
- Systematic and optimized control over the recording through simple and complex triggers
- FPGA based firmware allows updates for new technologies

PowerProbe

- 64 channels with 100 MHz, 32 channels with 200 MHz, 16 channels with 400 MHz
- State (external clock) recording of 100 MHz with up to 32 channels
- 256 K transient records
- 9 bit pattern generator, pulse generator
- FPGA trace



FPGA TRACE

Many of today's embedded designs involve FPGAs with embedded cores. The FPGA trace extension of the PowerProbe provides the ability to perform a simultaneous debugging of a processor's software and a FPGA based hardware.

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