TRITON-TX
electromechanical description and implementation guidelines

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Concept

The TRITON-TX is a Single-Board-Computer that integrates all the core components of a common PC and is mounted onto an application specific carrier board. TRITON-TX modules have a standardized form factor of 67,6mm x 26mm and have specified pinouts and provides the functional requirements for an embedded application. These functions include, but are not limited to, graphics, network and multiple USB ports. A single ruggedized SO-DIMM connector provides the carrier board interface to carry all the I/O signals to and from the TRITON-TX module. This SO-DIMM connector is a well known and proven high speed signal interface connector that is commonly used for memory cards in notebooks.

Carrier board designers can utilize as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly, TRITON-TX applications are scalable, which means once a product has been created there is the ability to diversify the product range through the use of different performance class TRITON-TX modules. Simply unplug one module and replace it with another, no redesign is necessary.

Disclaimer

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Intended Audience

This TRITON-TX electromechanical description is intended for technically qualified personnel. It is not intended for general audiences.

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Acronyms and Abbreviations

Abbreviation	Explanation
100-Base-T	Ethernet type that uses 100 Mega bits per second speed on RJ45 connectors and twisted pair wiring
ARM	Advanced RISC Machines Limited CPU architecture
JTAG	Joint Test Action Group. This abbreviation is commonly used to refer to a test interface found on many modern integrated circuits. The JTAG test interface is a boundary scan register with serial interface and is described by an IEEE standard
GPIO	General Purpose Input/Output
LCD	Liquid Crystal Display
LED	Light Emitting Diode. An electronic component used as a visual indicator (light).
NC	Not connected
PCB	Printed Circuit Board
RAM	Random Access Memory
RoHS	Restriction on Hazardous Substances: The Directive on the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment 2002/95/EC.
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

Table of contents

1 Feature Overview

TRITON-TX modules offers the newest I/O technologies on a minimum size form factor. This includes serial high speed buses such as:

- Ethernet
- USB
- SD - Secure Digital Card
- SPI - Serial Peripheral Interface

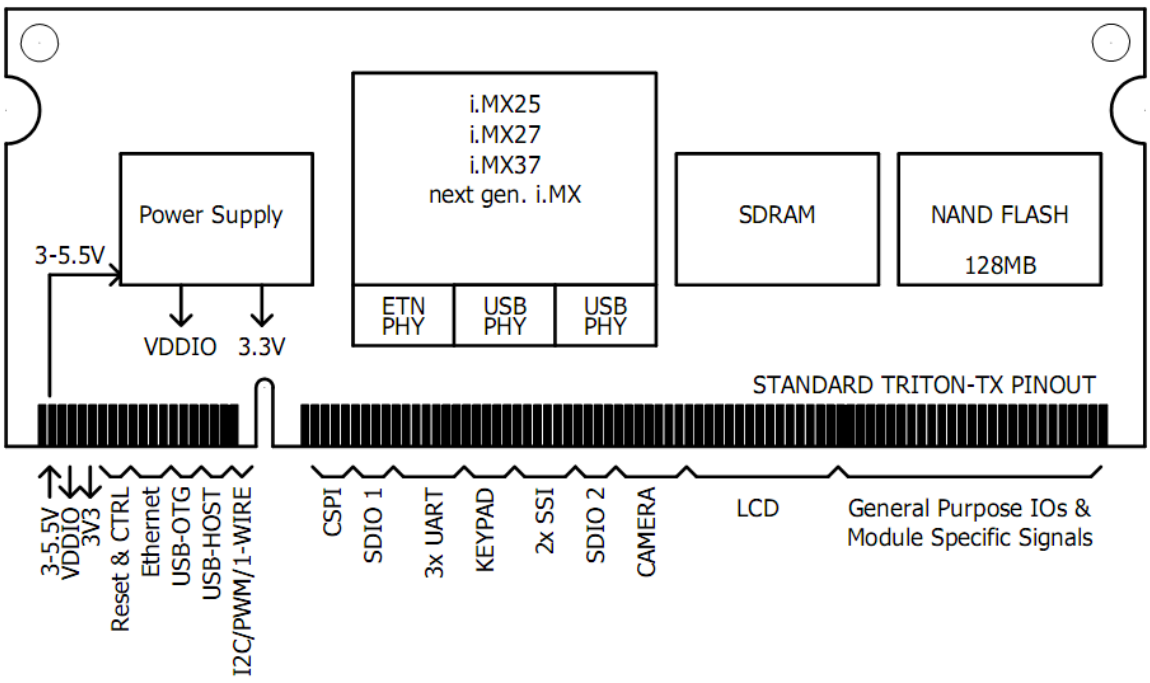
Multimedia interfaces

- CMOS Sensor Interface
- LCD True Color Display Interface (24bpp)

Other Standard Interfaces

- UART - Universal Asynchronous Receiver/Transmitters
- I2C - Inter-Integrated Circuit
- PWM - Pulse-Width Modulator
- 1-WIRE Interface

Plus additional control and power management signals. The versatile power supply outputs can also be used for the baseboard and defines the IO voltage used for the module. 1.8V and 3.3V IO voltage modules can be used on universal baseboards like the Starterkit V without the need for any change on the baseboard or jumper setting.



2 Connector Pin Assignments and Signal Descriptions

Signal names beginning with a "#" symbol indicates that the active, or asserted state, occurs when the signal is at a low voltage level. When "#" is not present, the signal is asserted when at a high voltage level. Differential pairs are indicated by trailing 'P' and 'N' for the positive or negative signal.

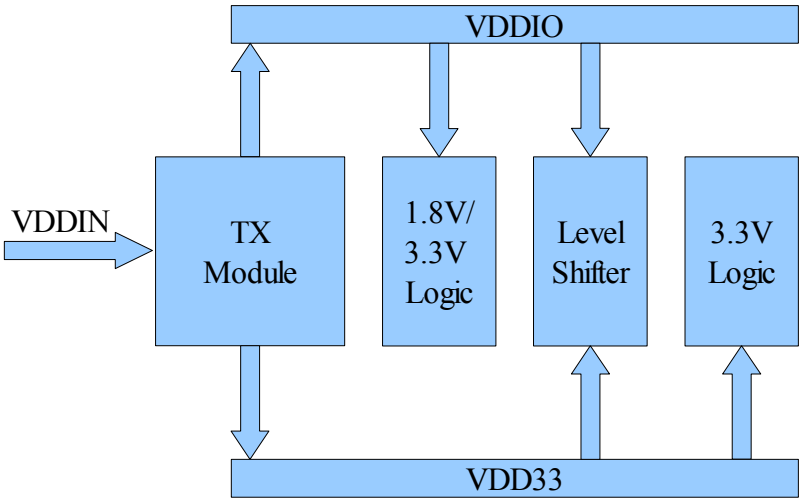
The following terminology is used to describe columns for the tables located below.

Term	Describtion
I	Input
O	Output
I/O	Bi-directional Input/Output Pin
VDDIO	I/O type depends on the VDDIO voltage of the module
3V3	I/O type: CMOS 3.3V
5V	I/O type: CMOS 3.3V to 5V
power	Power supply pin
USB	Universal Serial Bus differential pair signals In compliance with the Universal Serial Bus Specification 2.0
ETN	Ethernet Media Dependent Interface differential pair signals. In compliance with IEEE 802.3ab 100Base-T Ethernet Specification.
NC	Not Connected
PU	Pull-up resistor

2.1 Power Supply

<table>
<tr><th>Pin</th><th>Signal</th><th>Description</th><th>type</th><th>I/O</th></tr>
<tr><td>1-4</td><td>VDDIN</td><td colspan="2">Module power supply input</td><td>power</td><td>I</td></tr>
<tr><td>5-7</td><td>VDDIO</td><td colspan="2">1.8V or 3.3V I/O Power supply output
This output can be used for the module side supply of level shifters or for peripherals which are operated at the VDDIO voltage level.
Module | Remark
TX27,TX37 | VDDIO=1.8V / max. 900mA
TX25 | VDDIO=3.3V / VDDIO and VDD33 are connected on the module / max. 500mA</td><td>power</td><td>O</td></tr>
<tr><td>9-12</td><td>VDD33</td><td colspan="2">+3.3V Power supply output</td><td>power</td><td>O</td></tr>
<tr><td>18,26,32,39,
50,58,71,82,
88,94,102,
111,116,129,
142,147,160,
171,200</td><td>GND</td><td colspan="2"></td><td>power</td><td></td></tr>
</table>

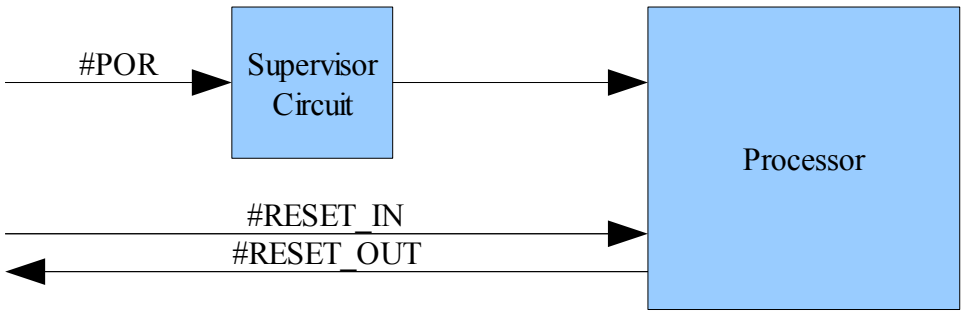
TX modules operates on a single 3.3V to 5.5V supply and provide regulated power supply outputs to the baseboard.



The use of level shifters on the baseboard to interface to 3.3V logic allows for universal module selection, because the voltage is automatically translated between VDDIO (1.8V or 3.3V) and VDD33 (3.3V) levels. Level shifters can be omitted on 3.3V only modules like the TX25, but in that case it's not possible to use 1.8V modules any more.

2.2 Reset & Bootmode

Pin	Signal	Description	type	I/O
8	BOOTMODE	System Boot Mode Select - The operational system boot mode of the module upon system reset is determined by the settings of this pin. BOOTMODE=H: Boot from NAND / L: Boot from UART/USB **Leave open or connect to VDDIO if not used.** **Module** / **Remark** TX27 / This signal is directly connected to VDDIO on version 1 and 2.	VDDIO PU	I
15	#RESET_OUT	Reset Out – Reset carrier board peripherals #RESET_OUT may be used to reset peripherals on the carrier board. Depending on the module type this signal might be asserted automatically by a system reset, but can be controller by a GPIO function during runtime on all modules.	VDDIO	O
16	#POR	Power On Reset - active low input signal. Typically a push button reset, pull low to force a reset. A supervisor circuit is used on the TRITON-TX module to monitor the power supply. This device assert a processor system reset (POR_B) if the power supply falls outside the programmed threshold or a manual reset (#POR) is asserted externally. **Connect to VIN or leave open if not used.** **Module** / **Remark** TX27 / A 100k pullup to VIN and 100nF to GND is needed to ensure proper power-up. Don't keep #POR active during power-up.	5V PU	I
17	#RESET_IN	Master Reset - external active low Schmitt trigger input signal. When this signal goes active, all modules (except the reset module, SDRAMC module, and the clock control module) are reset. The behaviour might depend on the processor, please refer to the processor reference manual for details. #RESET_IN is directly connected to the processors RESET_B pin. **Pull or connect to VDDIO if not used.**	VDDIO	I



2.3 RTC & Power-Button

Pin	Signal	Description	type	I/O
13	VBACKUP	RTC backup power supply. Supply voltage must be held between 1.3V and 3.7V for proper RTC operation. This pin can be connected to a primary cell such as a lithium button cell. Additionally, this pin can be connected to a rechargeable cell or a super cap when used with the trickle charge feature.		I
		Module / **Remark**		
		TX25 / DRYICE backup power supply input, max. 1.55V		
14	PMIC_PWR_ON	This is an active high push button input which can be used to signal PWR_ON and PWR_OFF events to the CPU by controlling the PMIC ext_wakeup signal and select contents of PMIC register 8H'88.		I
		Module / **Remark**		
		TX25 / Unused / Not connected		

2.4 Ethernet Signals

Pin	Signal	Description	type	I/O
19 21	ETN_TXN ETN_TXP	100Base-TX or 10Base-T differential transmit output to magnetics.	ETN	O
20	#ETN_LINKLED	Active low LINK ON indication: Active indicates that the link is on.	3V3	O
22	ETN_3V3	+3.3V analogue power supply output to magnetics. This power supply can be turned off on the module to reduce the power consumption in the case Ethernet is not needed.	power	O
23 25	ETN_RXN ETN_RXP	100Base-TX or 10Base-T differential receive input from magnetics.	ETN	I
24	#ETN_ACTLED	Active low ACTIVITY indication: Active indicates that there is Carrier sense (CRS) from the active PMD.	3V3	O

Tabelle 1: Ethernet Signals

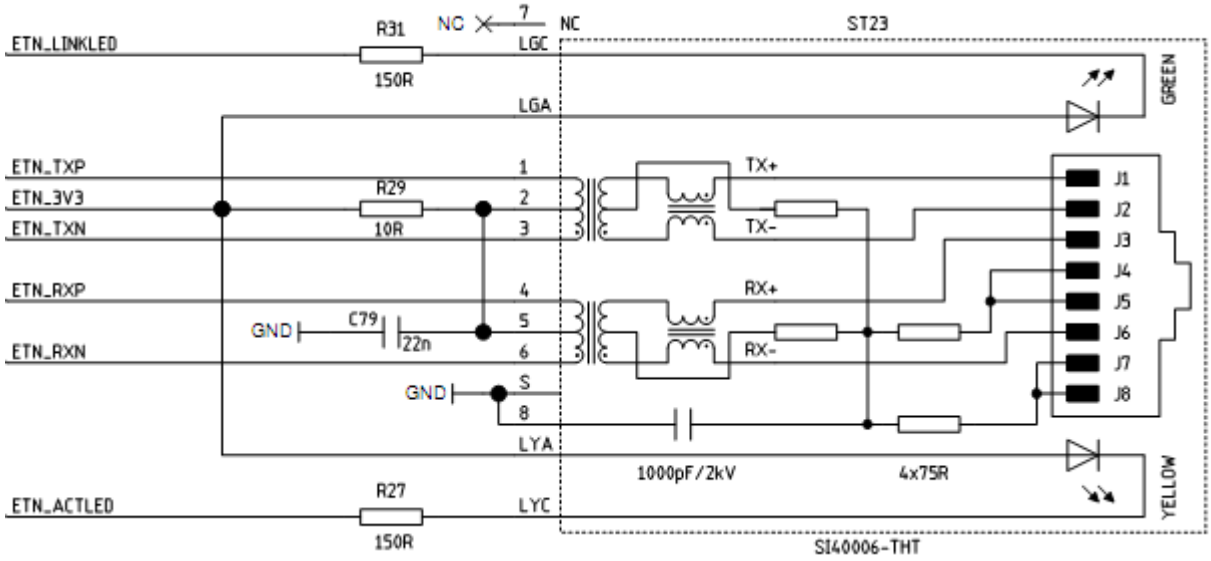


Abbildung 2.1: Ethernet Sample Diagram

2.4.1 Ethernet Physical Layer Layout Guidelines

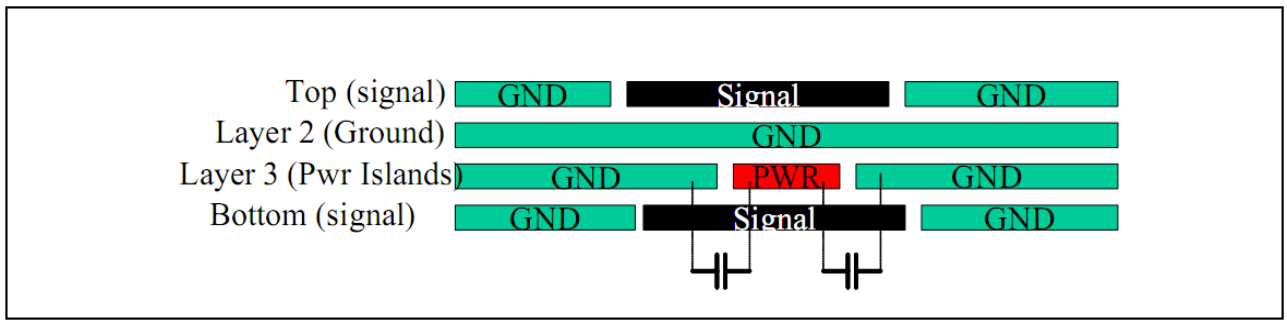
TRITON-TX modules are designed for 10 or 100 Mbps Ethernet systems. They are based on IEEE 10BASE-T and 100BASE-TX standards. The IEEE 802.3-2005 standard for 100BASE-TX defines networking over two pairs of Category 5 unshielded twisted pair cable or Type 1 shielded twisted pair cable. The following recommendations for the printed circuit board layout are not the only way to layout TRITON-TX modules. Every board designer will have a preference. Complexity, board space, number and types of devices will dictate routing and placement strategies.

2.4.2 Power and Ground Planes

The sections below describe typical 2 and 4 layer board stackups. The goal of the 4 layer designs is to keep the signal routing on outer layers, isolated by the power and ground planes. These power and ground planes also serve the purpose of reference planes for the signal traces. The signal traces should run over continuous reference planes when possible. When 2 layer board designs are required, it remains necessary that the signal traces run over continuous reference planes when possible.

2.4.3 4 Layer Stackup

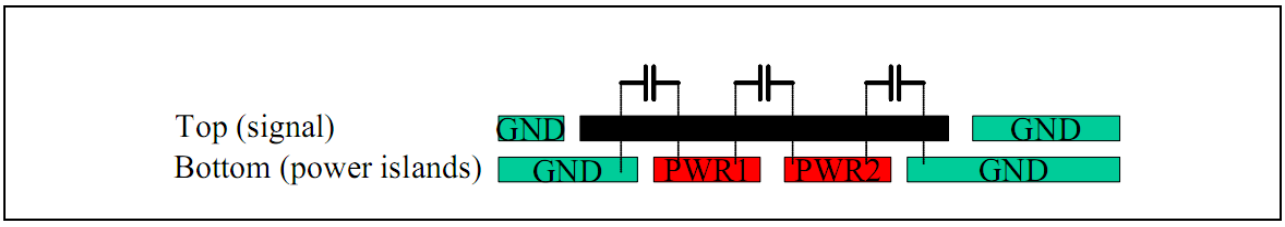
- TOP (Layer 1) – Signal with ground plane except where noted.
- Layer 2 – Continuous ground plane. No signals should be routed on this layer.
- Layer 3 – Power planes with ground planes except where noted. Signals may be routed on this layer if needed.
- Bottom (Layer 4) – Signal with ground plane except where noted.
- Decouple ground floods and ground layer as practical. When signal traces are re-referenced to power island planes, decoupling capacitors (10nF ceramic) are required between the ground plane and power plane.
- Signal traces routed on bottom layer over power islands that are on Layer 3 layer should have decoupling capacitors (10nF ceramic) near the trace to enable short (direct) return current paths.
- When signal traces are re-referenced to power island planes, decoupling capacitors (10nF ceramic) are required between the ground plane and power plane as shown below.



2.4.4 2 Layer Stackup

- TOP (Layer 1) – Signal with ground plane except where noted.
- Bottom (Layer 1) – Ground plane and power islands. A limited number of slow speed signals may be routed on the bottom layer.
- Signal traces should be surrounded by ground or ground trace along at least one edge. If ground trace is used, it should be connected to ground plane on this layer and decoupled to ground plane on top layer.
  Decouple ground planes as practical , as shown below. This will allow short (direct) return current paths when signal traces are re-referenced to different power island

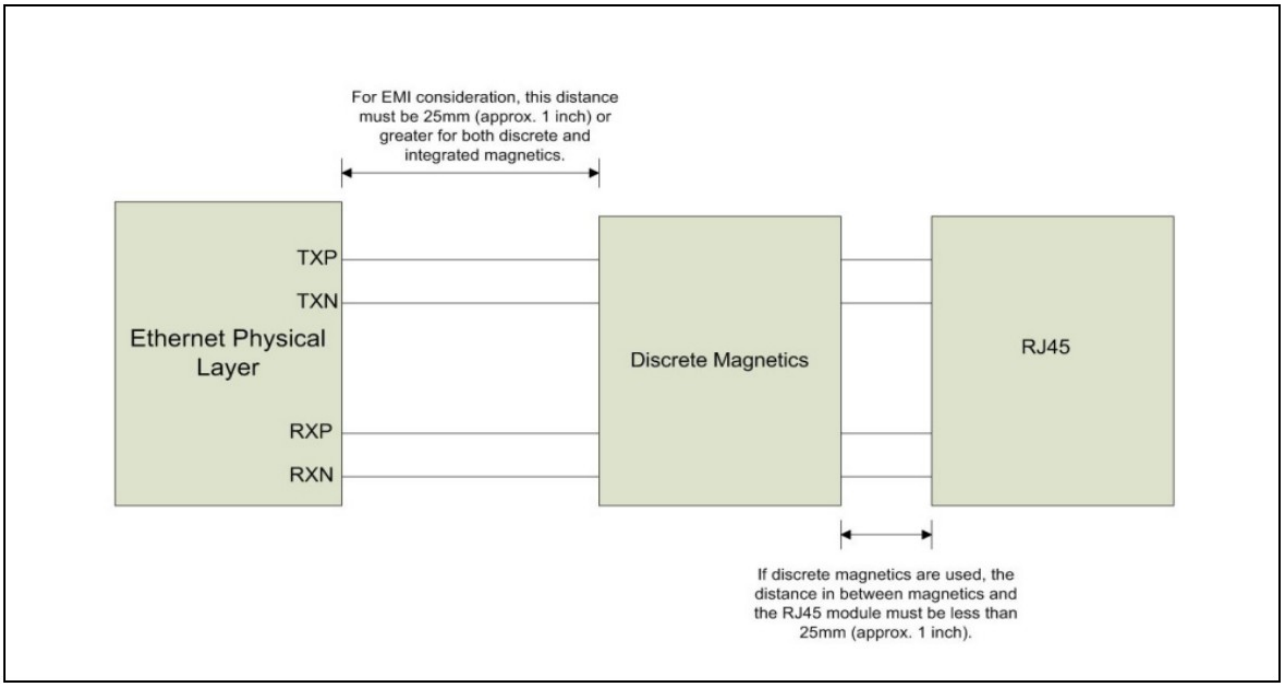
planes.



2.4.5 Component Placement

Component placement can affect signal quality, emissions, and component operating temperature. Careful component placement can decrease potential EMI problems and simplify the task of routing traces.

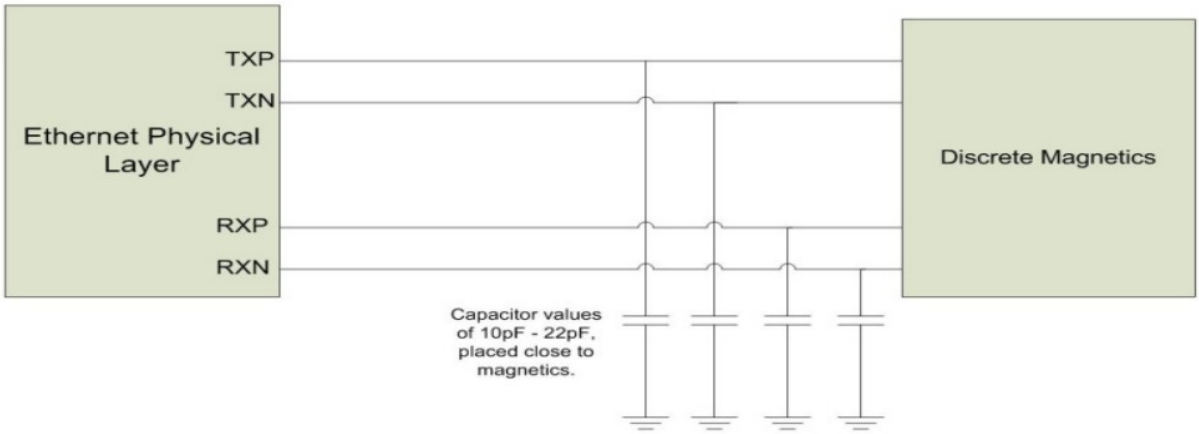
- If the magnetic is a discrete component, then the distance between the magnetic and the RJ-45 needs to have the highest consideration and be kept to under 25mm (approx. 1 inch) of separation.
- The distance between the SO-DIMM socket and the magnetics needs to be 20mm or greater. Among PHY vendors, the 25mm (approx. 1 inch) rule is considered good design practice for EMI considerations. The intention is to isolate the PHY from the magnetics.



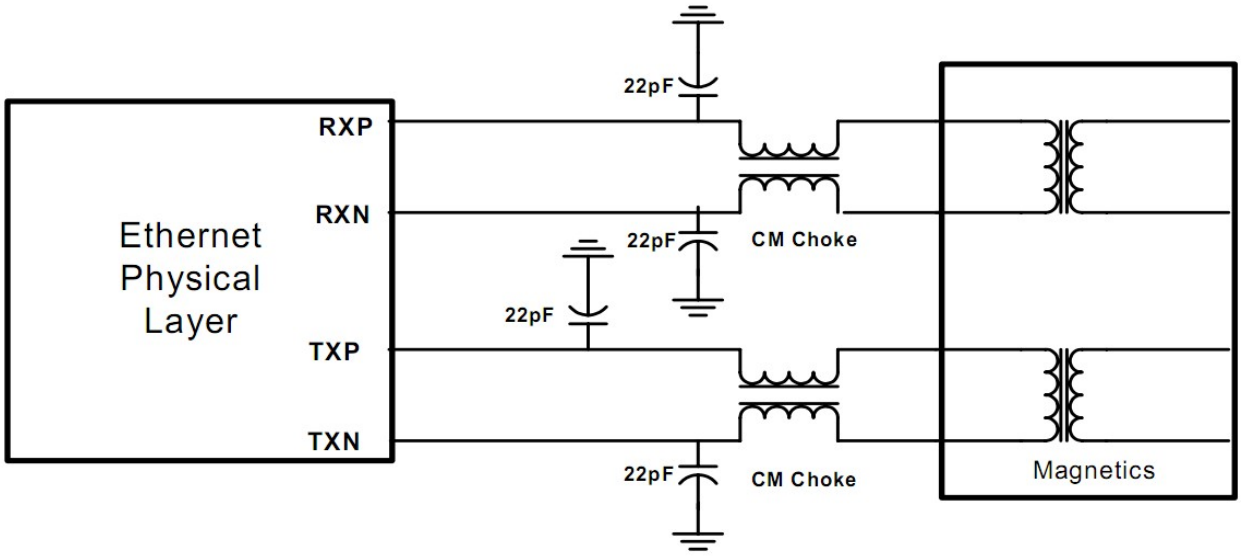
2.4.6 Design Techniques for EMI Suppression

The following techniques may improve EMI margin.

- Common mode capacitors may be added to the TX+/- and RX+/- signals for high frequency attenuation , as shown below. One end of each capacitor should be connected to the system ground plane, and placed within 10mm (approx. 400mils) of the magnetics. Typical capacitance values should be between 10pF and 22pF. Values higher than 22pF may negatively impact the TX and RX signalling.

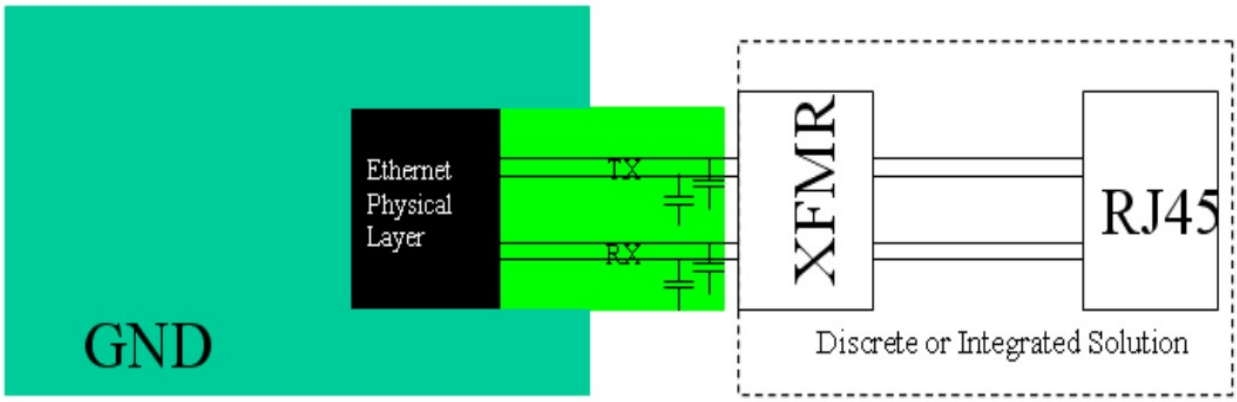


- Common mode chokes may be added to the TX and RX differential pairs as shown below. The common mode chokes should be placed within 10mm (approx. 400mils) of the integrated RJ45 module, and on the magnetics side of the common mode EMI suppression capacitors. Typical common mode impedance of the common mode choke selected should be 2kΩ@100MHz or higher.



- In general, no ground plane should extend under the TX and RX differential pairs, under the magnetics, or under the RJ45 jack. In the case where common mode capacitors used for EMI suppression, a ground plane may be located under the TX and RX signals, however the plane must not exceed beyond the capacitors. When designing 4 layer boards, the ground plane should exist on layer 4, assuming the differential pair is routed on layer 1. On 2 layer boards, the ground plane can be located on layer 2, the adjacent layer to the TX and RX signal pairs. Under no circumstances should a ground plane exist under the magnetics, the RJ45 connector or in between the magnetics and RJ45 connector.

2.4.7 Controlled Impedance for Differential Signals



The 802.3-2005 specifications requires the TX and RX lines to run in differential mode. The TXP and TXN are a differential pair and need to be designed to a 100 ohm differential impedance. The RXP and RXN traces are also a differential pars and need to be designed to a 100 ohm differential impedance target.

The board designer must maintain 100 ohm differential impedance in the layout for all differential pairs. For differential dielectric thickness, copper weight or board stack-up, trace width and spacings will need to be calculated.

Differential pair nets must maintain symmetry. TXP and TXN must be equal length and symmetric with regards of shape, length, and via count. RXP and RXN must also be equal length and symmetric.

Isolation of TX/RX traces. The TX/RX traces must be isolated from nearby circuitry and signals. Maintain a distance of parts to lines that are greater than or equal to 5 times the distance of the spacing between the traces. Do not route differential pairs under parts. Do not cross TX/RX lines with other PCB traces unless the traces are on the opposite side of the ground plane from TX/RX.

2.4.8 Magnetics Module

The magnetics module has a critical effect on overall IEEE and emissions conformance. The device should meet the performance required for a design with reasonable margin to allow manufacturing variation. Occasionally, components that meet basic specifications may cause the system to fail IEEE testing, because of interactions with other components or the Printed Circuit Board itself. Carefully qualifying new magnetics modules can go a long way toward preventing this type of problem.

Suggested magnetics have not been tested in order to verify proper operation. This category of magnetic has been evaluated by the contents of the vendor supplied data sheet and legacy performance only. However, the designer can assume with some degree of confidence, that with proper PCB design techniques, the magnetics presented as suggested magnetics will perform to high standards.

Qualified magnetics have been tested by the PHY vendor in order to verify proper operation. The designer can assume with a high degree of confidence, that with proper PCB design techniques, the qualified magnetics perform to the highest standards.

Vendor	Part Number	Package	Temp	Status
Pulse	H1102	16-pin SOIC	0°..+70°C	Qualified
Halo	TG110-RP55N5	16-pin SOIC	0°..+70°C	Qualified
Halo	HFJ11-RP26E-L12RL	Integrated RJ45	0°..+70°C	Qualified
Delta	RJSE1R5310A	Integrated RJ45	0°..+70°C	Qualified
Pulse	J0011D01B	Integrated RJ45	0°..+70°C	Suggested
Bothhand	TS6121C	16-pin SOIC	0°..+70°C	Suggested
Bothhand	LU1S041X-43	Integrated RJ45	0°..+70°C	Suggested
Pulse	HX1102	16-pin SOIC	-40°..+85°C	Qualified
Halo	TG110-RPE5N5	16-pin SOIC	-40°..+85°C	Qualified
Halo	HFJ11-RPE26E-L12RL	Integrated RJ45	-40°..+85°C	Qualified
TDK	TLA-6T717W	Integrated RJ45	-40°..+85°C	Qualified
Delta	LFE8505T	16-pin SOIC	-40°..+85°C	Qualified
Midcom	000-7090-37R	16-pin SOIC	-40°..+85°C	Suggested
Midcom	MIC66211-5171T-LF3	Integrated RJ45	-40°..+85°C	Suggested
Elec & Eltek	820-M0323R	16-pin SOIC	-40°..+85°C	Suggested

2.5 USB

Pin	Signal	Description	type	I/O
27 34	USBH_VBUSEN USBOTG_VBUSEN	This pin is used to enable the external VBUS power supply.	3V3	O
28 36	#USBH_OC #USBOTG_OC	Active low over-current indicator input connected to a GPIO. This signal can be used as an input only.		I
30 38	USBH_VBUS USBOTG_VBUS	VBUS pin of the USB cable. This pin is used for the VBUS comparator inputs.	5V	I
31 29	USBH_DP USBH_DM	USB Host port differential data signal	USB	I/O
37 35	USBOTG_DP USBOTG_DM	USB OTG port differential data signal	USB	I/O
33	USBOTG_ID	ID pin of the USB cable. For an A-Device ID is grounded. For a B-Device ID is floated. Tie this pin to GND for the USB-OTG port to be used as a 2nd host port.		I

Module	Remark
TX25	USBH_VBUS unused / Not connected
TX37	USBH USB host port unused / Not connected

2.5.1 USB Physical Layer Layout Guidelines

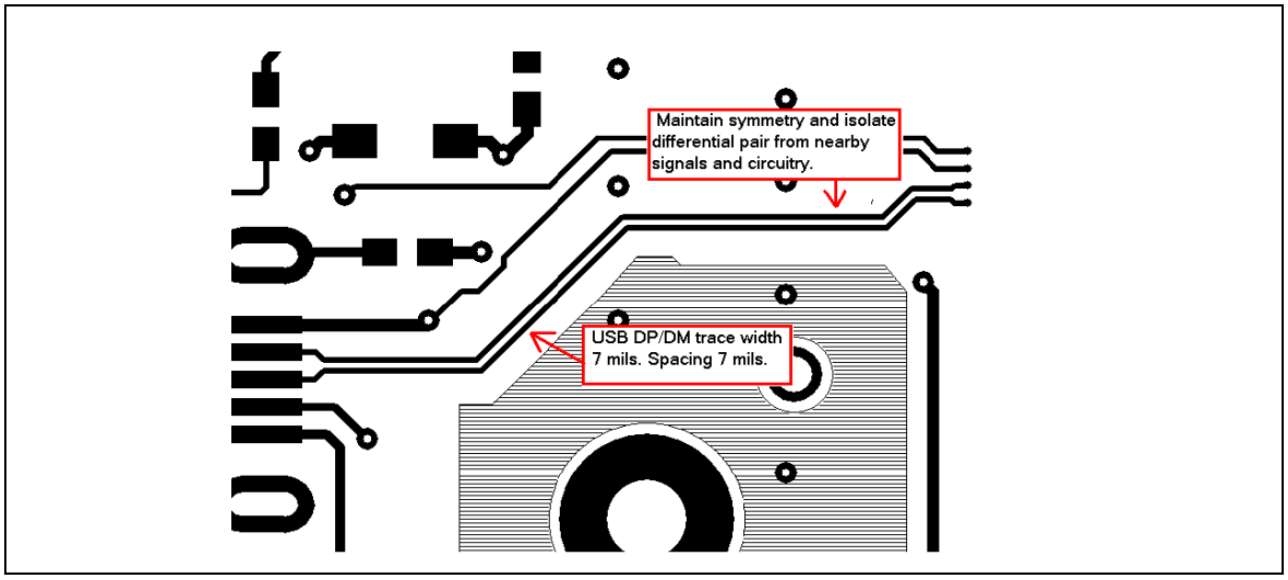
The TRITON-TX modules includes the physical layer interface (PHY) for systems using Hi-Speed USB. Proper design techniques must be used in printed circuit board (PCB) layout to maintain the signal integrity required for 480 Mbps operation.

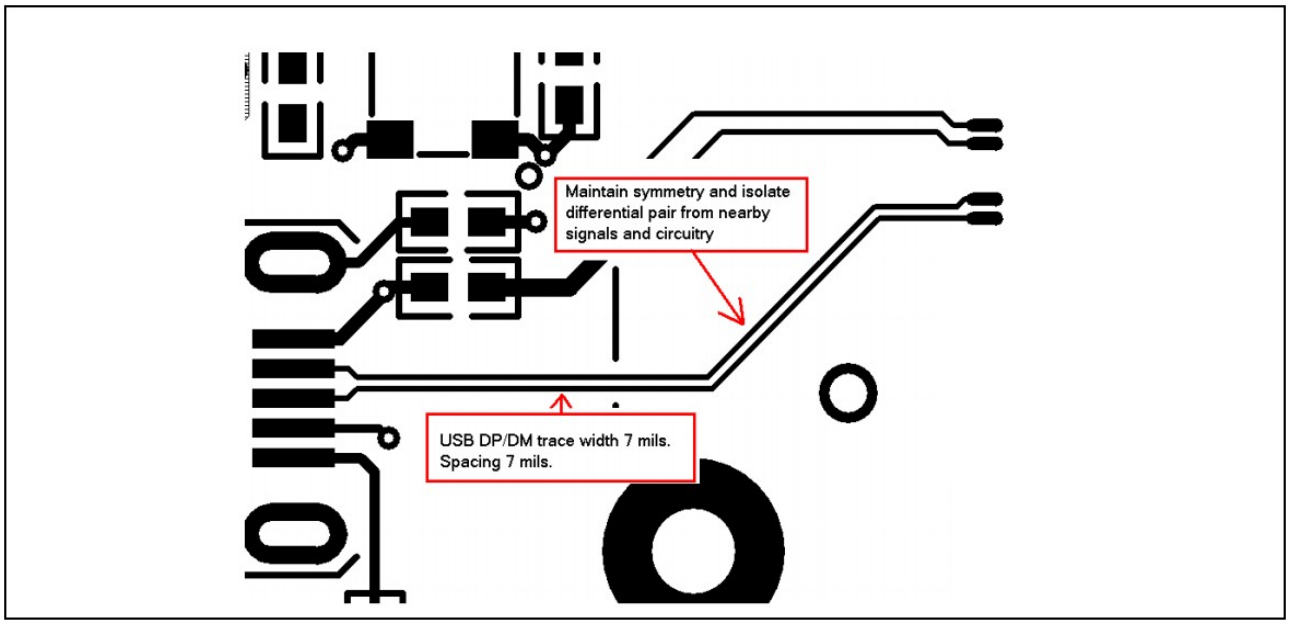
2.5.2 Controlled Impedance for USB Traces

the USB 2.0 specification requires that the USB DP/DM traces maintain a nominal 90 Ohms +/- 15% differential impedance (see USB specification Rev. 2.0, paragraph 7.1.1.3 for more details). In the example design the traces are 7 mil (175um) wide with line spacing of 7 mils. These numbers are derived for 5 mil (125um) distance from ground reference plane. A continuous ground plane is required directly beneath the DP/DM traces and extending at least 5 times the spacing width to either side of DP/DM lines.

Maintain symmetry between DP/DM lines in regards to shape and length.

Single sided impedance is not as critical as differential impedance. A range of 42 to 78 Ohms is acceptable (equivalently, common mode impedance must be between 21 Ohms and 39 Ohms).



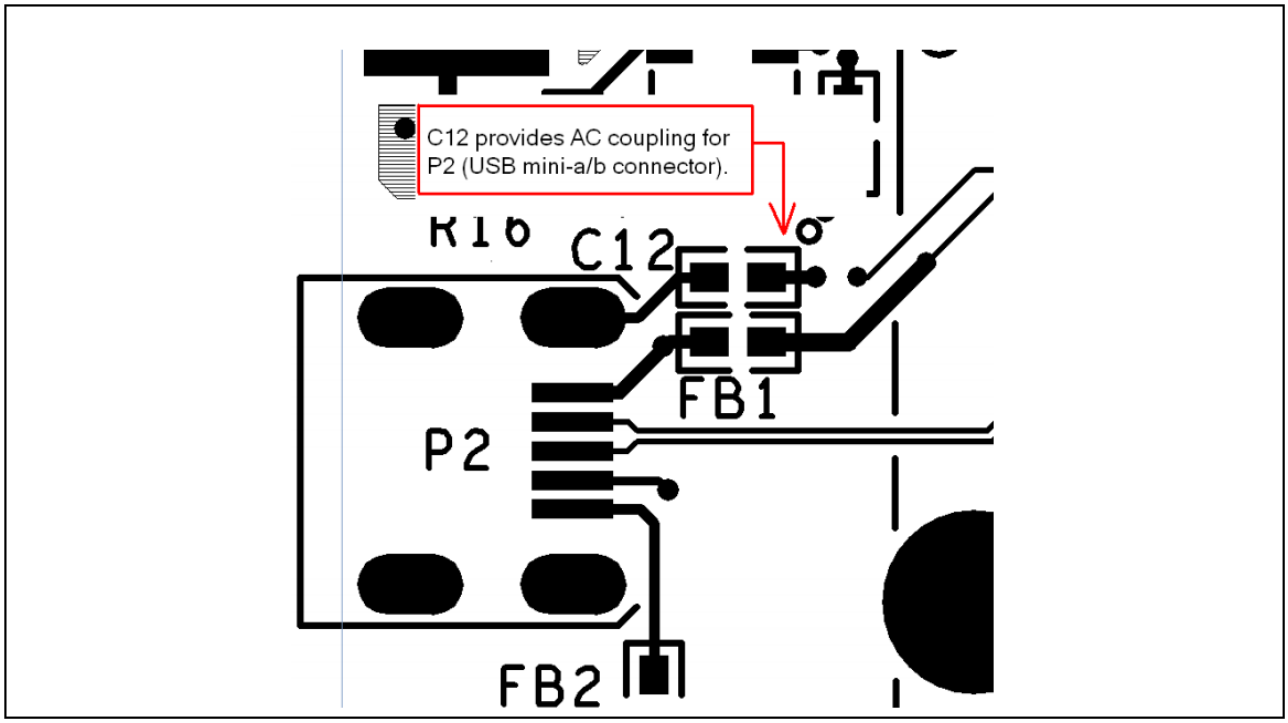


The figures show DP/DM traces with approximately equal trace length and symmetry. It is important to maintain a conductor width and spacing that provides differential and common mode impedance compliant with the USB specification. Use 45 degree turns to minimize impedance discontinuities.

2.5.3 Isolation of DP/DM Traces

The DP/DM lines must be isolated from nearby circuits and signals. Maintain a distance of components to lines that is greater or equal to 5 times the distance of the spacing between the traces. Do not route differential pairs under components. Do not cross DP/DM lines with other PCB traces unless the traces are on the opposite side of the ground plane from DP/DM. Route DP/DM over solid ground plane with no ground plane splits under the traces.

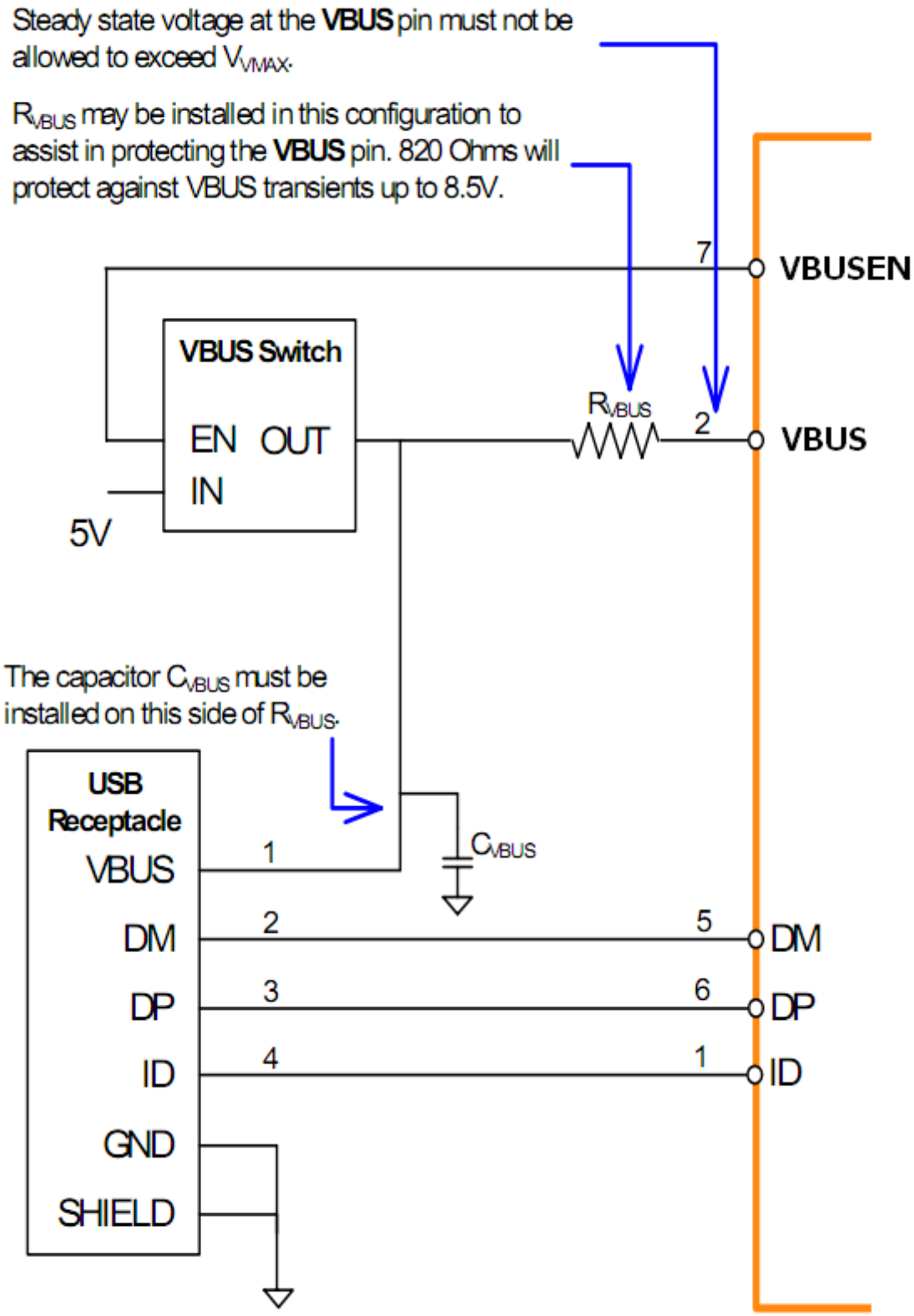
2.5.4 Isolated shielding on the USB connector



The figure shows the Mini-AB connector housing is isolated but AC coupled to the device ground. Industry convention is to ground only the host side of the cable shield. This is done to provide cable shielding while preventing possible ground currents from flowing in the USB cable if there happens to be a potential difference between the host and device grounds. If DC grounding is required replace C12 with a zero Ohms resistor.

In OTG applications the shield may be DC grounded at both ends of the cable.

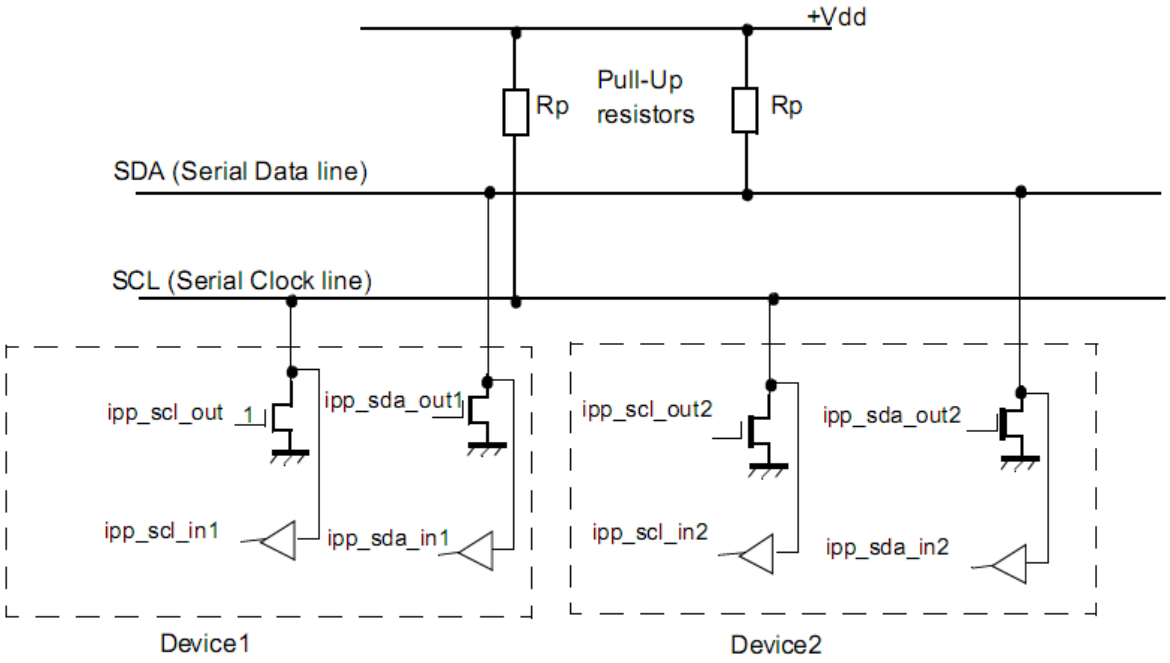
2.5.5 Optional VBUS protection



2.6 I2C

Pin	Signal	Description	type	I/O
40	I2C_DATA	I2C Data	VDDIO	I/O
41	I2C_CLK	I2C Clock	VDDIO	O

The I2C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices. The flexible I2C allows additional devices to be connected to the bus for expansion and system development.

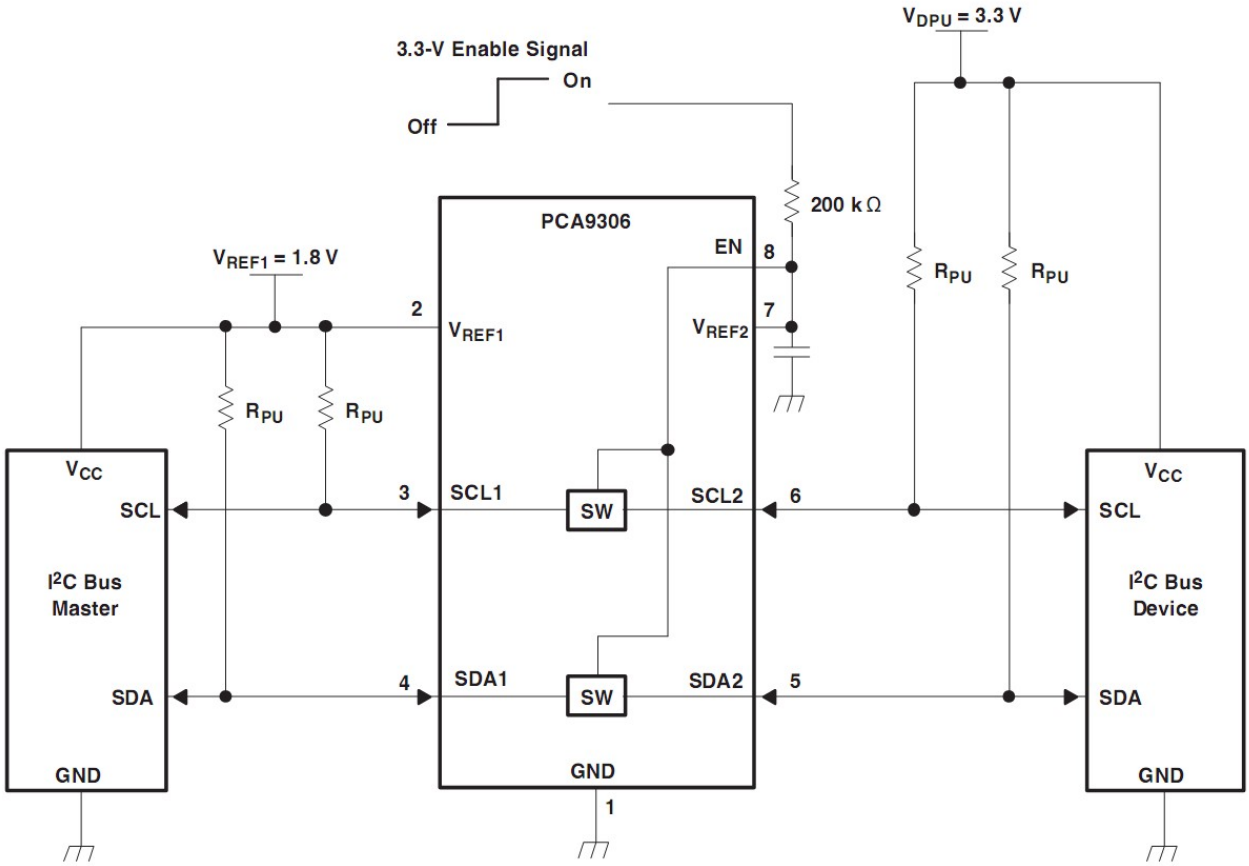


2.6.1 Example I2C Voltage Level Translator

The Texas Instruments PCA9306 allows bidirectional voltage translations between 1.2 V and 5 V, without the use of a direction pin.

As with the standard I2C system, pullup resistors are required to provide the logic high levels on the translator's bus. The PCA9306 has a standard open-collector configuration of the I2C bus. The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with standard-mode and fast-mode I2C devices, in addition to SMBus devices. Standard-mode I2C devices only specify 3 mA in a generic I2C system where standard-mode devices and multiple masters are possible. Under certain conditions, high termination currents can be

used.



PULLUP RESISTOR VALUES(1)(2)

PULLUP RESISTOR VALUE (Ω)						
V_{DPU}	15 mA		10 mA		3 mA	
	NOMINAL	+10%(3)	NOMINAL	+10%(3)	NOMINAL	+10%(3)
5 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312

(1) Calculated for V_{OL} = 0.35 V
(2) Assumes output driver V_{OL} = 0.175 V at stated current
(3) +10% to compensate for V_{DD} range and resistor tolerance

2.7 PWM / 1-WIRE

Pin	Signal	Description		type	I/O
42	PWM	Pulse-Width Modulator (PWM) Output		VDDIO	O
		Module	**Remark**		
		TX37	Unused / Not connected		
43	OWIRE	1-Wire		VDDIO	I/O

1-Wire is a registered trademark of Dallas Semiconductor for a device communications bus systems designed by Dallas Semiconductor that provides low-speed data, signalling and power over a single signal, albeit using two wires, one for ground, one for power and data. 1-Wire is similar in concept to I2C, but with lower data rates and longer range. It is typically used to communicate with small inexpensive devices.

2.8 CSPI – Configurable Serial Peripheral Interface

Pin	Signal	Description	type	I/O
44	CSPI_SS0	Slave Select bidirectional, selectable polarity signal, output in master mode, and input in slave mode.	VDDIO	I/O
45	CSPI_SS1		VDDIO	I/O
46	CSPI_MOSI	Master Out Slave In bidirectional signal, which is TxD output signal from the data shift register in master mode. In Slave mode it is RxD input to the data shift register.	VDDIO	I/O
47	CSPI_MISO	Master In Slave Out bidirectional signal, which is RxD input signal to the data shift register in master mode. In Slave mode it is TxD output from the data shift register.	VDDIO	I/O
48	CSPI_SCLK	CSPI Clock bidirectional signal, which is CSPI clock output in master mode. In slave mode it is an input CSPI clock signal.	VDDIO	I/O
49	CSPI_RDY	Serial Data Ready signal - This input signal is used for hardware control only in master mode. It indicates that external SPI slave is ready to receive data. It will edge or level trigger a CSPI burst if used. If the hardware control enabled, CSPI will transfer data only when external SPI slave is ready	VDDIO	I/O

Module	Remark
TX37	No CSPI interface available, used for TV-Out instead

The i.MX processors contains Configurable Serial Peripheral Interface (CSPI) modules that allow rapid data communication with fewer software interrupts than conventional serial communications. Each CSPI is equipped with two data FIFOs and is a master/slave configurable serial peripheral interface module, allowing processor to interface with both external SPI master and slave devices.

2.9 SDIO Interfaces

Pin	Signal	Description	type	I/O
51, 95	SD1_CD SD2_CD	SD Card Detect – connected to a GPIO	VDDIO	I
52, 96	SD1_D[0] SD2_D[0]	SD Data bidirectional signals	VDDIO	I/O
53, 97	SD1_D[1] SD2_D[1]			
54, 98	SD1_D[2] SD2_D[2]			
55, 99	SD1_D[3] SD2_D[3]			
56, 100	SD1_CMD SD2_CMD	SD Command bidirectional signal	VDDIO	I/O
57, 101	SD1_CLK SD2_CLK	SD Output Clock.	VDDIO	O
Module		**Remark**		
TX25		Only one SD-Card available, SD Interface 2 is not used / not connected		

The TX pinout provides two dedicated SDIO interfaces. SDIO stands for Secure Digital Input Output which can also be used for SD-Memory-Cards.

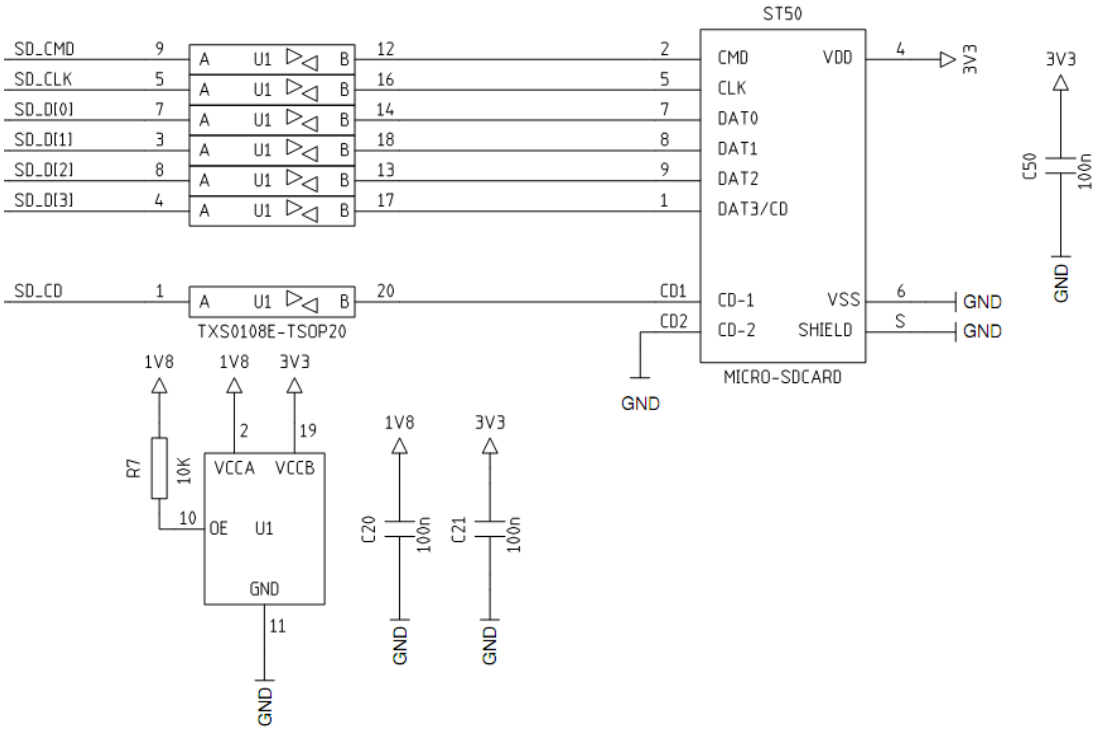


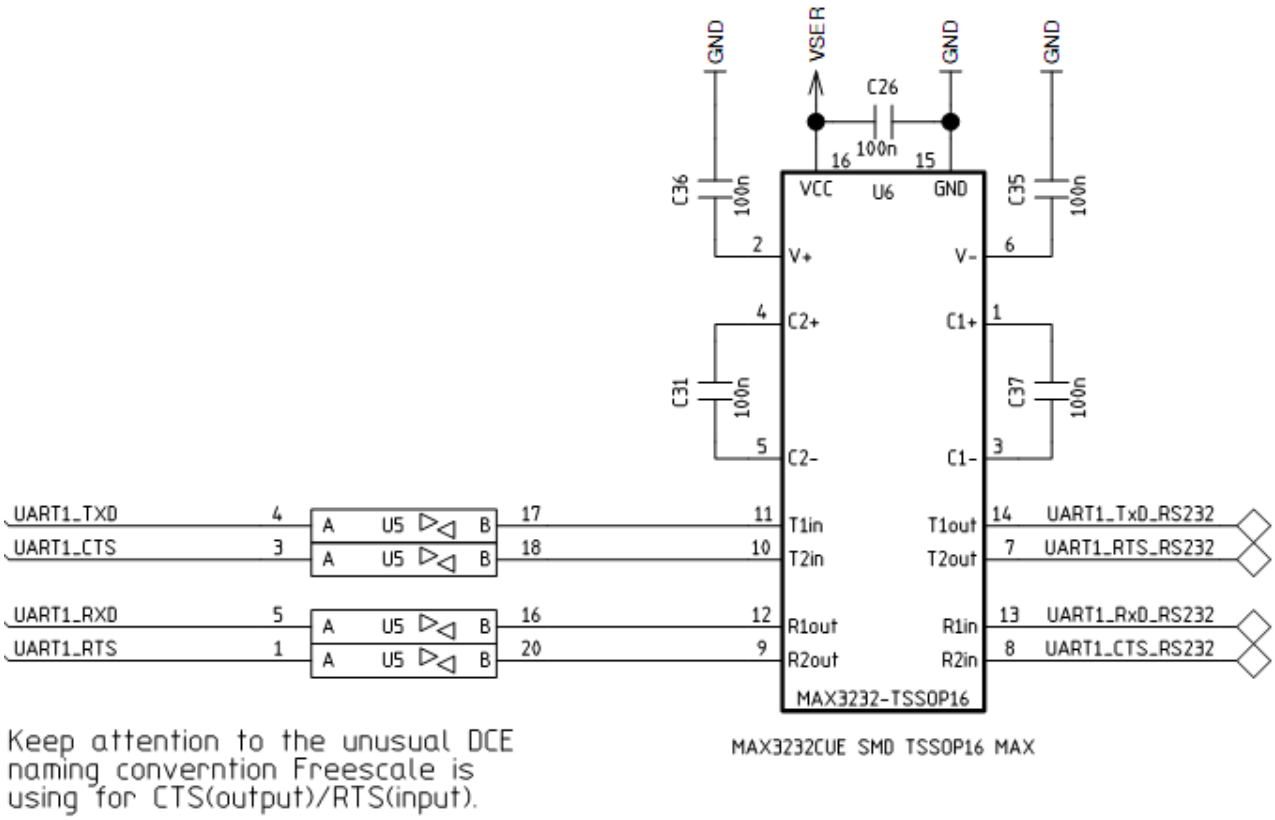
Abbildung 2.2: SD-Card Example diagram

Pullup Resistors
Each port of the TXS0108E has an internal pull-up resistor. These have a value of 40 kΩ when the output is driving low and a value of 4 k Ω when the output is driving high.

2.10 UARTs

Pin	Signal	Description	type	I/O
59, 63, 67	UART1_TXD UART2_TXD UART3_TXD	Transmit Data output signal	VDDIO	O
60, 64, 68	UART1_RXD UART2_RXD UART3_RXD	Receive Data input signal	VDDIO	I
61, 65, 69	UART1_RTS UART2_RTS UART3_RTS	Request to Send input signal	VDDIO	I
62, 66, 70	UART1_CTS UART2_CTS UART3_CTS	Clear to Send output signal	VDDIO	O
Module		**Remark**		
TX37		Supports only 2 UARTs, UART3 not used / not connected		

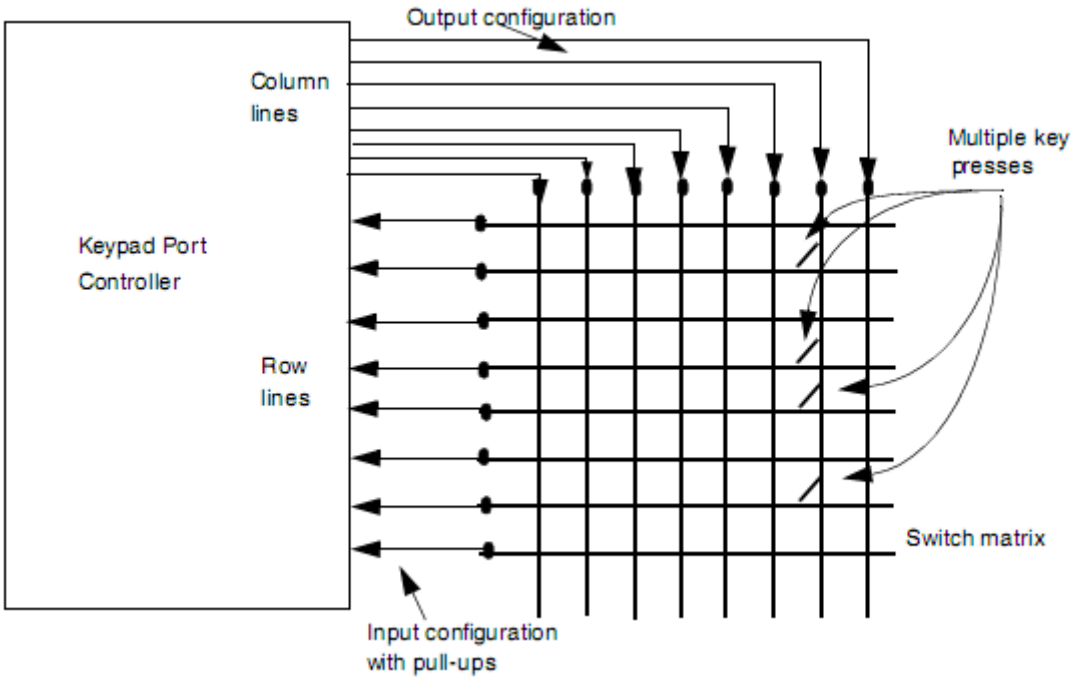
2.10.1 UART Example diagram



2.11 Keypad Interface

Pin	Signal	Description	type	I/O
72	KP_COL[0]	Keypad Column selection signals.	VDDIO	
73	KP_COL[1]		VDDIO	
74	KP_COL[2]		VDDIO	
75	KP_COL[3]		VDDIO	
76	KP_COL[4]		VDDIO	
77	KP_ROW[0]	Keypad Row selection signals.	VDDIO	
78	KP_ROW[1]		VDDIO	
79	KP_ROW[2]		VDDIO	
80	KP_ROW[3]		VDDIO	
81	KP_ROW[4]		VDDIO	
Module		**Remark**		
TX37		KP_COL[3], KP_COL[4], KP_ROW[4] not used / not connected		

The Keypad Port (KPP) is designed to interface with the keypad matrix with 2-point contact or 3-point contact keys. The KPP is designed to simplify the software task of scanning a keypad matrix. With appropriate software support, the KPP is capable of detecting, debouncing, and decoding one or multiple keys pressed simultaneously on the keypad.



2.12 Digital Audio Ports

Pin	Signal	Description	type	I/O
83 89	SSI1_INT SSI2_INT	Interrupt		
84 90	SSI1_RXD SSI2_RXD	Receive serial data		
85 91	SSI1_TXD SSI2_TXD	Transmit serial data		
86 92	SSI1_CLK SSI2_CLK	Serial clock		
87 93	SSI1_FS SSI2_FS	Frame Sync		
Module		**Remark**		
TX37		SSI2 not used / not connected		

The SSI is a full-duplex, serial port that allows the chip to communicate with a variety of serial devices. These serial devices can be standard CODer-DECoder (CODECs), Digital Signal Processors (DSPs), microprocessors, peripherals, and popular industry audio CODECs that implement the inter-IC sound bus standard (I2S) and Intel AC97 standard.

SSI is typically used to transfer samples in a periodic manner. The SSI consists of independent transmitter and receiver sections with independent clock generation and frame synchronization.

2.13 CMOS Sensor Interface

Pin	Signal	Description	type	I/O
103-110	CSI_D[0-7]	Sensor port data		
112	CSI_HSYNC	Sensor port horizontal sync		
113	CSI_VSYNC	Sensor port vertical sync		
114	CSI_PIXCLK	Sensor port data latch clock		
115	CSI_MCLK	Sensor port master clock		

Module	Remark
TX37	CMOS Sensor Interface not used / not connected

The CMOS Sensor Interface (CSI) enables the chip to connect directly to external CMOS image sensors. CMOS image sensors are separated into two classes, dumb and smart. Dumb sensors are those that support only traditional sensor timing (Vertical SYNC and Horizontal SYNC) and output only Bayer and statistics data, while smart sensors support CCIR656 video decoder formats and perform additional processing of the image (for example, image compression, image pre-filtering, and various data output formats).

The CSI can support to connect one 8-bit sensor.

2.14 LCD Interface

Pin	Signal	Description	type	I/O
117-128, 130-141	LCD_D[0-23]	LCD Data		
143	HSYNC	Line Pulse or HSync		
144	VSYNC	Frame Sync or VSync—This signal also serves as the clock signal output for gate; driver (dedicated signal SPS for Sharp panel HR-TFT)		
145	OE_ACD	Alternate Crystal Direction/Output Enable		
146	LSCLK	Shift Clock		

The LCD Controller of the i.MX processors provides display data for external greyscale or color LCD panels. The LCD Controller is capable of supporting black-and-white, greyscale, passive-matrix color (passive color or CSTN), and active-matrix color (active color or TFT) LCD panels.

The TRITON-TX LCD Interface defines a generic 24 bit Panel Interface LCD_D[23..0]. The TFT color channel assignments are shown in the table below:

LCD_D	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TX37	LD 23	LD 22	LD 21	LD 20	LD 19	LD 18	LD 17	LD 16	LD 15	LD 14	LD 13	LD 12	LD 11	LD 10	LD 9	LD 8	LD 7	LD 6	LD 5	LD 4	LD 3	LD 2	LD 1	LD 0
TX25 TX27	LD 17	LD 16	LD 15	LD 14	LD 13	LD 12	GP IO	GP IO	LD 11	LD 10	LD 9	LD 8	LD 7	LD 6	GP IO	GP IO	LD 5	LD 4	LD 3	LD 2	LD 1	LD 0	GP IO	GP IO
24bpp	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	G7	G6	B5	B4	B3	B2	B1	B0
18bpp	R5	R4	R3	R2	R1	R0			G5	G4	G3	G2	G1	G0			B5	B4	B3	B2	B1	B0		
16bpp	R4	R3	R2	R1	R0				G5	G4	G3	G2	G1	G0			B4	B3	B2	B1	B0			
12bpp	R3	R2	R1	R0					G3	G2	G1	G0					B3	B2	B1	B0				

With this assignment the two module types – 18bpp like the TX25 and TX27 and 24bpp like the TX37 – can be used on the same carrier board without any change. On 18bpp modules the unused bits are always connected to General Purpose IOs to be able to drive these to a defined level.

2.15 GPIO and module specific signals

Pin	Signal	Description	type	I/O
148-159	GPIO[0-11]	General Purpose Input/Output **Module** / **Remark** TX37: Only GPIO[5] on pin 153 is available. The other GPIOs are unused / not connected	VDDIO	I/O
161-170, 172-182, 184-199		Module specific interfaces – refer to datasheet for details		

3 Optional Debugging Connector

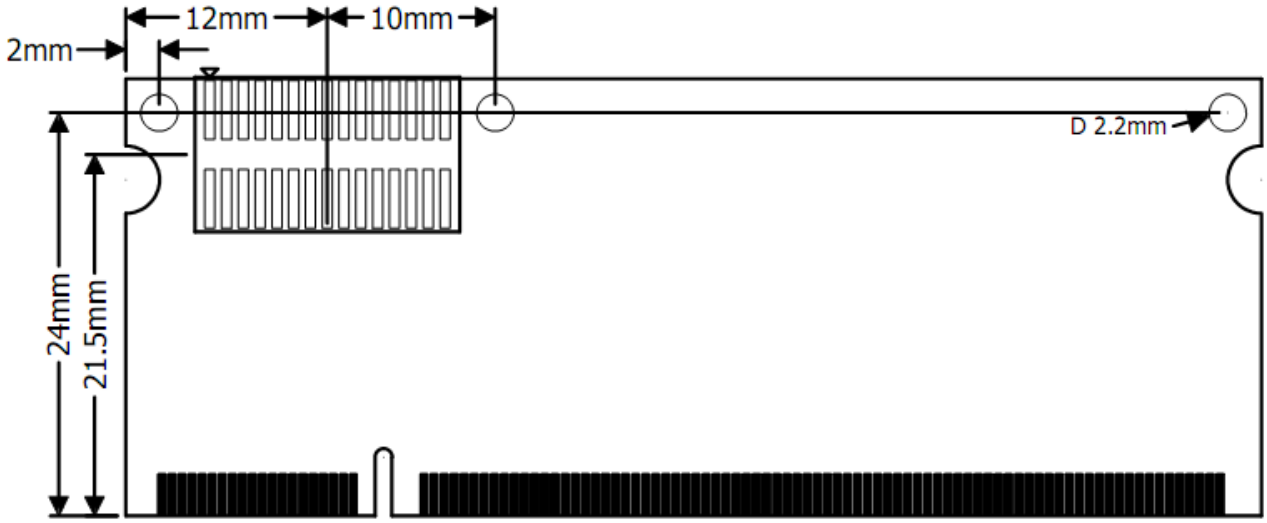
3.1 Debug Connector Signal Assignment

Pin	Signal	Description	type	I/O
1	MFG_NC1	Do not connect on the carrier board. These pins are reserved for manufacturing purposes.		
3	MFG_NC0			
5	BOOT[1]	Module specific boot mode, refer to table below or the processor datasheet. Boot from flash is selected, if these pins are not connected.	VDDIO	I
7	BOOT[0]		VDDIO	I
9	GND			
11	#TRST		VDDIO	
13	TMS		VDDIO	
15	TDO		VDDIO	
17	TDI		VDDIO	
19	GND			
21	TCK		VDDIO	
23	GND			
25, 27, 29	NC			
2, 4, 6 … 28, 30	GND			

3.2 Boot mode selection

Boot from	TX25	TX27	TX37
NAND	BOOT[1,0]=	BOOT[1,0]=10	BOOT[1,0]=10
Serial UART/USB	BOOT[1,0]=	BOOT[1,0]=00	BOOT[1,0]=11

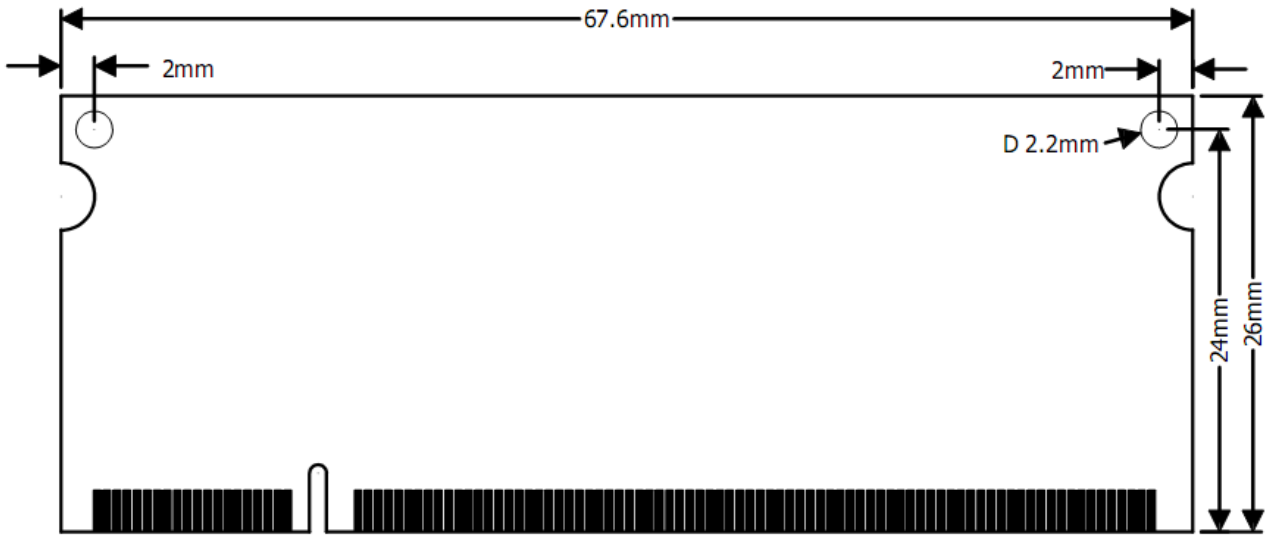
3.3 Debug connector location

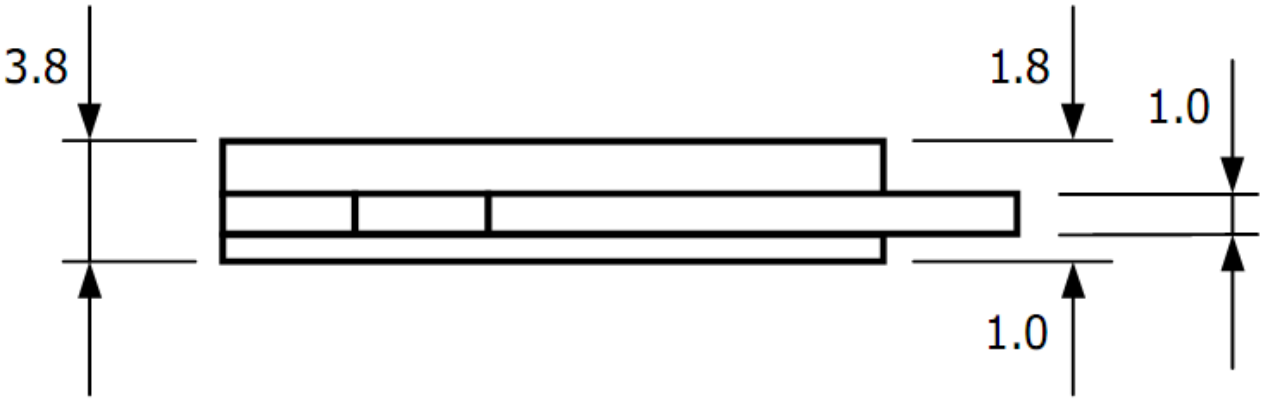


Mates with Samtec FSI - 3mm Height, One Piece Interface, part no. FSI-115-03-G-D-AD
The SO-DIMM connector socket height has to be 5.2mm if the debug connector is used.

4 Mechanical

4.1 TRITON-TX module outline





4.2 SO-DIMM connector

For detailed information on socket dimensions and recommended PCB layout refer to the manufacturer datasheets. Be sure to use DDR SO-DIMM type sockets with 2,5V keying.

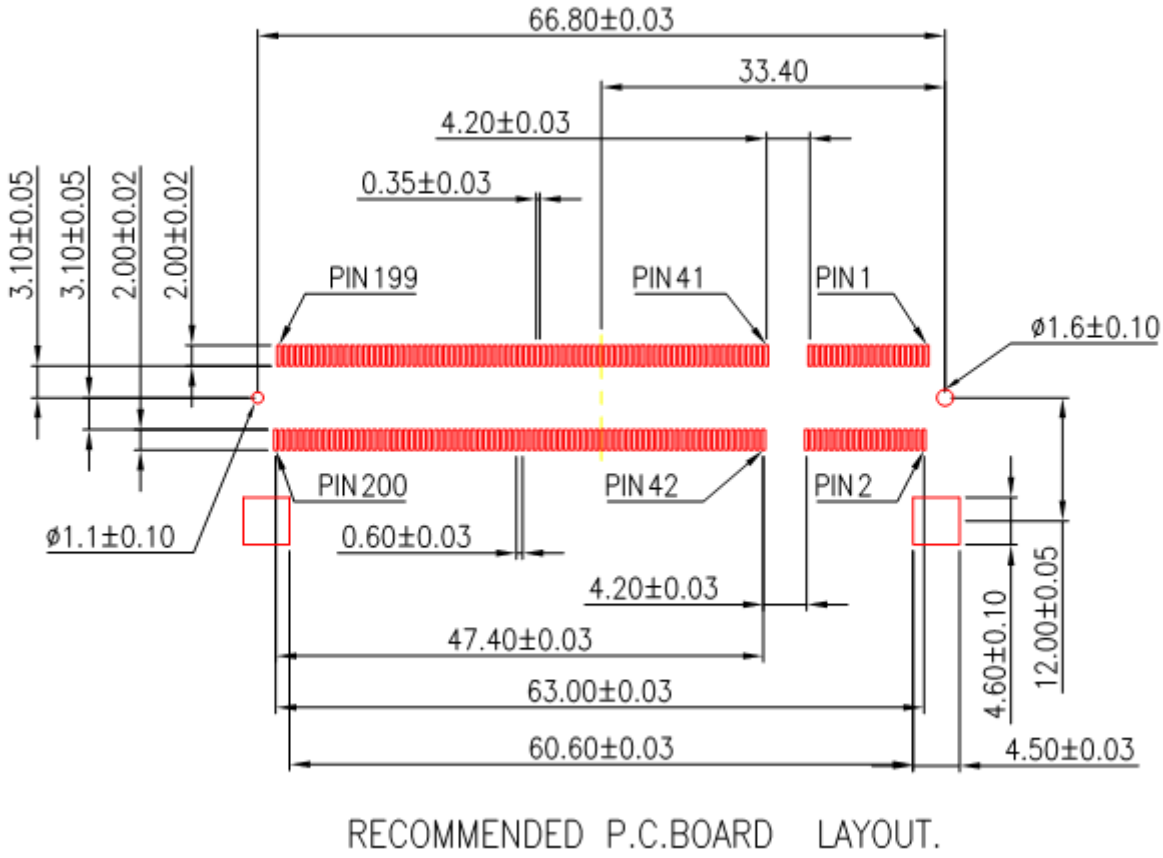
Part number	Socket height	Overall mounting height	Underside space	Supplier
1565691-1	4,0mm	4,5mm	0,5mm	Tyco Electronics
AS0A426-E4SN-7F				Foxconn
SODIMM200S52T25	5,2mm	5,7mm	1,7mm	admatec
AS0A426-E2SN-7F				Foxconn
1473005-1				Tyco Electronics
AS0A426-B6SN-7F	6,5mm	7,0mm	3,0mm	Foxconn
1717468-3				Tyco Electronics
AS0A426-B8SN-7F	8,0mm	8,5mm	4,5mm	Foxconn
SODIMM200S92T25	9,2mm	9,7mm	5,7mm	admatec
AS0A426-EASN-7F				Foxconn

Tabelle 2: SO-DIMM part numbers and suppliers

Typical DDR SO-DIMM Socket specifications

- Durability : 25 Cycles
- Voltage Rating: 25V
- Current Rating: 0.3A
- Contact Resistance: 50mΩ max.
- Dielectric Withstanding Voltage: 250V AC/1 min.
- Insulation Resistance: 100MΩ
- Operating Temperature: -40°C to +85°C

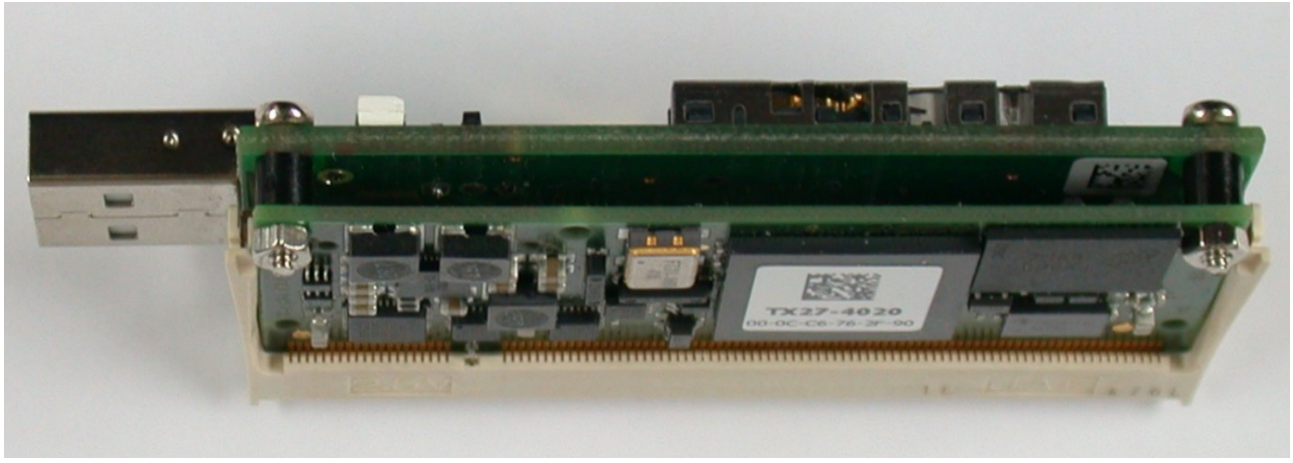
4.3 Recommended DIMM Connector PCB Layout example



4.4 Ruggedized SO-DIMM

A fastener kit provides secure mounting of modules plugged into the SO-DIMM socket. An additional thread locker is recommended to hold the screws in during vibration.

Ka-Ro Part number	Description	Quantity
MEK:812-0540	Self Retaining Screw Spacer for M2,0 Length 3,0 mm, Outside Diameter 4,00 mm www.ettinger.de part. no. 07.51.403 	2
MEK:812-0355	Nut M2,0	2
MEK:812-0354	Screw M2,0 x 8mm	2



5 Document Revision history

Revision	Changes
2009-05-28	Initial release
2009-07-21	ETN_RXN, ETN_RXP wrong pin mapping corrected.